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Feasibility Study for Radio Frequency Transistors and Monolithic Integrated Circuits up to 10GHz with Application to Launch Vehicle's Communication Systems

Telemetry, Data Link, Beacon and Transponder Systems

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Preface

The present document reports an study on the feasibility aspects for designing and manufacturing microwave power transistor and/or power amplifiers monolithic integrated circuits (MMICs) up to 12.4GHz for electronics of communications equipments to be used in Argentinian space launch vehicles.
The work is divided in ten chapters, chapters one to seven are the so called Deliverable Documents. These chapters are grouped in four deliverable documents. The chapter seven contains the final conclusions of the current report. Chapter eight to ten were added to support the feasibility study with the aim to self contain a widespread number of topics involved in the subject under study.
This work was carried out at LAPSyC and GISEE Laboratories at Universidad Nacional del Sur and supported by VENG-CONAE.
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Contents

List of Figures

Chapter 1

Specifications Analysis (First Deliverable Document)

This chapter describes and analyzes the requirements and specification for high power microwave transistors and power amplifiers required for CONAE's launch vehicle communication systems. The information is organized as follows: first, the specifications for the communication systems are analyzed. Parameters such as power, efficiency, modulation, bandwidth and frequency for the required standards are specified. In addition, an analysis of the power budget for all the amplifying chain (namely from the amplifier to the antenna) is addresses to assess the suitability of possible design alternatives. Namely, if is required integration of single transistors, transistors with matching networks included, array of multiple transistors in parallel, or integration of a complete amplifier circuit.
Second, the specification for Radiation Tolerance and Reliability are analyzed. This section includes the study of standards and requirements of radiation tolerance for the transmitter systems and the required levels of reliability in their components.
Finally, a comparative table with requirements is presented for quick reference.

1.1 Specifications

1.1.1 Standard for Telemetry & Data Link

Telemetry specifications are based on Telemetry Standard RCC Document 106-9 [1]. These standard provide the criteria to determine equipment and frequency use requirements and are intended to ensure efficient and interference-free use of the frequency spectrum.

1.1.1.1 Output Microwave Power

Emitted power levels (power at load) shall always be limited to the minimum required for the application, but in any case shall not exceed 25W. The specifications required by CONAE are 10 W of output power at load.

1.1.1.2 Efficiency, Operating Class & Linearity

Power added efficiency of 40% is required for this application. Thus, AB or C amplifier classes shall be used. In turns, the conducting angle (how deep in AB or C class is the power amplifier biased) shall be related to the linearity specification which is given in terms of third order inter-modulation distortion [27].
Continuous wave transmitting systems are quite robust to non linear effects, even those that use multilevel digital phase or frequency modulation. The standard do not specify the linearity requirement in terms of Bit Error Rate (BER) or Error Vector Magnitude (EVM), in its place specify (as a measure of linearity) that the inter-modulation products at lateral bands do not shall exceed -25dBm. The inter-modulation products considered are only those related with 3rd order products. The power or bandwidth (were -25dBm is founded)are calculated using equation A-10 (from Appendix A [1]). See next two sections for details on these concepts.

1.1.1.3 Modulation

The modulation methods for aeronautical telemetry are frequency modulation and phase modulation. CONAE has specified the use of digital FM modulation (CPFSK/FM). Other methods can be used when better bandwidth efficiency is required. Table 1.1 also shows the modulation methods included in the telemetry standard. This table shows the relative bandwidth as a function of the transmitted digital bit rate.

Modulation Method	Bandwidth
CPFSK (PCM/FM) [28]	1.16.Bit Rate
FQPSK-B (Feher) [29]	0.78.Bit Rate
FQPSK-JR (Feher) [29]	0.78.Bit Rate
SOQPSK-TG [30]	0.78.Bit Rate
ARTM CPM [31]	0.56.Bit Rate

Table 1.1: Telemetry Modulation Methods and their theoretical relative bandwidths

1.1.1.4 Frequency allocation & Bandwidths

Allocation frequency for telemetry in this project are in the lower S-band (2200-2290 MHz) and in the upper S-band (2310-2390 MHz). Lowest frequency are shared equally by the United State Government´s fixed, mobile, space research, space operation, and the Earth exploration-satellite services. These frequencies include telemetry associated with launch vehicles, missiles, upper atmosphere research rockets, and space vehicles regardless of their trajectories. Upper frequencies are allocated for fixed, mobile, radio location, and broadcasting-satellites in the United State of America. Telemetry assignments are made for flight-testing of manned or unmanned aircraft, missiles, space vehicles, or their major components.
In previous section we mentioned that transmission bandwidth depends on the modulation scheme and the transmitted bit data rate. There are three bit data rate to be considered: 1Mbits, 5Mbits and 20MBits. The telemetry standard defines the required bandwidth for a bit rate in terms of spectrum power using the -25dBm output power rule (see Appendix A [1]). This rule states that the required bandwidth is the bandwidth containing all components larger than -25dBm measured at the transmitter output (see Figure 1.1).

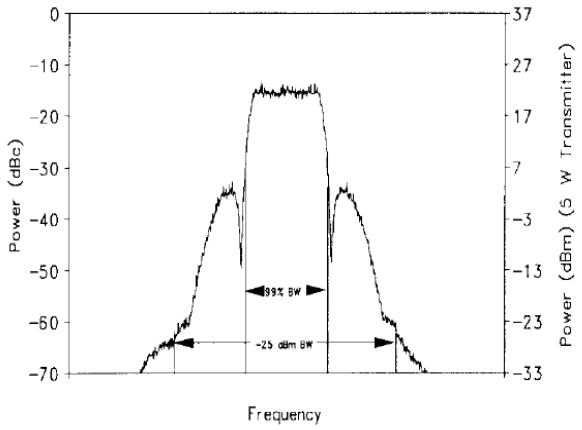


Figure 1.1: -25dBm Measurement of a RNRZ PCM/FM signal (From [1])

Tables 1.2, 1.3 and 1.4 shows the calculated bandwidth required for each modulation and data rates using the -25dBm rule. These calculations were done using equation A-10 of Appendix A of [1].

Modulation Method	1MBits	5MBits	20MBits
CPFSK (PCM/FM)	4.38MHz	18.62MHz	64.86MHz
FQPSK-B (Feher)	3.04MHz	8.72MHz	30.34MHz
FQPSK-JR (Feher)	3.04MHz	8.72MHz	30.34MHz
SOQPSK-TG	3.04MHz	8.72MHz	30.34MHz
ARTM CPM	1.56MHz	6.60MHz	23.02MHz

Table 1.2: Transmission Bandwidth for 5Watt Transmitter using -25dBm Bandwidth Criteria

Modulation Method	1MBits	5MBits	20MBits
CPFSK (PCM/FM)	4.68MHz	19.78MHz	69.5MHz
FQPSK-B (Feher)	2.20MHz	9.34MHz	32.5MHz
FQPSK-JR (Feher)	2.20MHz	9.34MHz	32.5MHz
SOQPSK-TG	2.20MHz	9.34MHz	32.5MHz
ARTM CPM	1.66MHz	7.08MHz	24.66MHz

Table 1.3: Transmission Bandwidth for 10Watt Transmitter using -25dBm Bandwidth Criteria

Modulation Method	1MBits	5MBits	20MBits
CPFSK (PCM/FM)	5.14MHz	21.88MHz	76.20MHz
FQPSK-B (Feher)	2.40MHz	10.24MHz	35.64MHz
FQPSK-JR (Feher)	2.40MHz	10.24MHz	35.64MHz
SOQPSK-TG	2.40MHz	10.24MHz	35.64MHz
ARTM CPM	1.82MHz	7.76MHz	27.04MHz

Table 1.4: Transmission Bandwidth for 25Watt Transmitter using -25dBm Bandwidth Criteria

From tables 1.2, 1.3 and 1.4 we can determine the minimum bandwidth for a specific system design, being the worst case a system with CPFSK and 20MBits of data rate(76.20MHz).
Commercial products are commonly sold with 100MHz of bandwidth although not always the full bandwidth is used at time due to channelization aspects.

1.1.1.5 Maximum Load VSWR

Power amplifier must be specified to withstand a VSWR greater than the worst case expected at any phase angle over the entire frequency range.
A typical requirement [32] might be VSWR as great as **3:1**, which is half the power reflected. This specification considers that the power amplifier is connected to the antenna system by mean of a power coupler, thus the insertion losses of wires and coupler prevent the reflection of all power even in the worst case (antenna open or shorted). When the power amplifier is directly connected to the antenna

with a low loss transmission line, new values of VSWR (close to infinite) shall be considered.

1.1.1.6 Products for Reference

Below we present for reference a couple of featured products for telemetry. The list will be expanded and studied in detail in Chapter 3 to get better understanding of transistors and power amplifier specifications.

- L3 Communications: PA805S 5W Power amplifier [33].
- L3 Communications: PA220S 20W Power amplifier [34].

1.1.2 Standard for Transponder

Transponder specifications are based on Non-Coherent Radar Transponder Standard document RCC 262-02 [2]. This standard provide the criteria to determine equipment and frequency use requirements and is intended to ensure efficient and interference-free use of the frequency spectrum.

1.1.2.1 Output Microwave Power

The transmitter shall have or complies with three different power specifications: 20 watts, 50 watts or 400 watts of minimum peak output power. This power amplifier versions must operate with a pulse repetition of 10 pulses per second to 2600 pulses per second. The pulse duration shall be from 250 nseconds through 600 nseconds. There are other pulse's features defined by the standard such as 1.2: rise time, fall time, overshoot and drop. The last, the percentage of power drop at the end of the pulse is related with the thermal characteristics of the power amplifier. This value, around 6%, shall be carefully observed during study of thermal aspects of semiconductor process since is related to thermal time constant of the substrate [35].

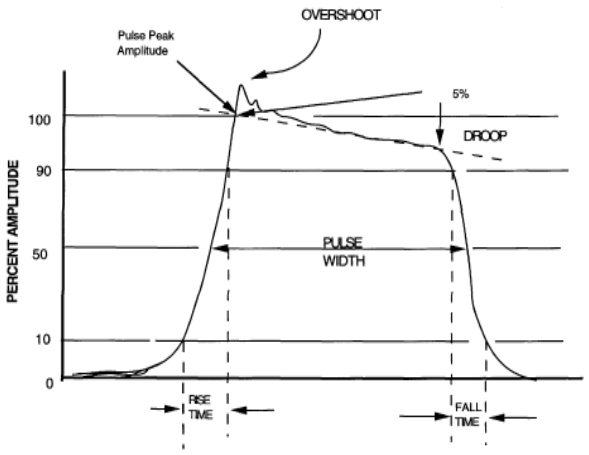


Figure 1.2: Pulse Waveform definition (From [2])

The average power dissipation is related with the duty cycle of the pulsed transmitter transmitter. As a worst case (the fast PRF and the long pulse) the average power is less than 1% of the peak output power.

1.1.2.2 Efficiency, Operating Class & Linearity

The standard do not defines the efficiency, operating class or linearity. Amplifiers at C or X bands are commonly biased either in class B or C [36]. This bias is preferred because the RF output power of the amplifier is maximized. From linearity point of view class B is preferred when low power must be handled. In class C the linear region only exist for 1dB to 3dB of the input dynamic range RF signal and shall be used for high power applications. It is clear that for both cases, class C and B, an output harmonic filter must be considered to limit the total harmonic distortion.

1.1.2.3 Frequency allocations & Bandwidth

The transponder set receives pulse type interrogating signals and transmits a pulse type signal in the same frequency band. The transponder is required to accept interrogation signals from single or multiple radar sets and provide a tracking pulse for specified band instrumentation radar sets. Frequencies specified in this standard have been determined as the frequency bands comprised by C-Band from 5.4GHz to 5.9GHz, and the the X-Band transponders with frequency bands between 8.4GHz to 9.0GHz and from 9.0GHz to 9.6GHz.
The required bandwidth is related with the pulse duration. The standard defines the spectrum as follow: The RF pulse spectrum measured at the 6 dB points, shall not exceed 1.7 divided by the pulse width (in MHz). The first side lobes shall be a minimum of 9 dB below the main, measured from peak to peak. The first nulls bordering the main lobe shall be spaced a nominal 2 divided by the pulse width (in MHz) apart and shall be a minimum of 12 dB below the peak of the main lobe.

A priori calculus give as a result that the worst case of bandwidth requirement (a pulse width of 250 nseconds)for a transponder implementation is roughly 7MHz. Current commercial products implements 100 nseconds transmitting pulse with a bandwidth of 15MHz [37].

1.1.2.4 Maximum Load VSWR

The transponder shall meet all requirements of the standard when operating into a mismatch, such as to cause a VSWR up to **2:1**, at any phase angle of the entire frequency range.

1.1.2.5 Products for Reference

Below we present for reference a couple of featured products. The list will be expanded and studied in detail in Chapter 3 to get better understanding of transistors and power amplifier specifications.

- L3 Communications: LT401, 200Watts C-Band Radar Transponder [37].

1.1.3 Standard for Beacon

These specifications are based on CONAE's requirements. We did not receive a specific standard for guidance from CONAE, but as we will see next, general beacon specifications are quite less demanding than telemetry and transponder systems.
We found several types of beacon systems that can fit in CONAE systems requirements. We will only mention both that can fit on launch vehicles operations.
First, does exist distress beacons systems for emergency and rescue [38]. Distress radio beacons are activated under emergency event to send out a distress signal that, when detected by non geostationary satellites, can be located by triangulation. There are three kinds of distress radio beacons:

- **EPIRBs:** Emergency Position Indicating Radio Beacons, signal maritime distress.
- **ELTs:** Emergency Locator Transmitters, signal aircraft distress.
- **PLBs:** Personal Locator Beacon, are for personal use and are intended to indicate a person in distress.

In second place, we have the Space and Radio Satellite beacons. They are used in both geostationary and inclined orbit satellites. Any satellite will emit one or more beacons whose purpose is two fold, send the telemetry information and send the satellite location (azimuth and elevation).

1.1.3.1 Output Microwave Power

Output power shall be at least in the order of 5W with a maximum of 15W. Exact value shall be decided with CONAE's project team.

1.1.3.2 Efficiency, Operating Class & Linearity

Efficiency of 40% or higher is required for this application. AB or C class should be used on power amplifiers. Due to low level modulations (BPSK or FSK) and pulsed operation higher efficiency levels better than 70% can be expected.

1.1.3.3 Frequency allocation & Bandwidth

Distress beacons (digital ones) works in 406MHz band with bandwidth requirement of less than 1MHz. Satellite beacons are customary operated at 1275 MHz and 1445 MHz bands with a 50 MHz bandwidth.

1.1.3.4 Other Requirements

- Power output should be protected against open/short load.
- Transmitter should count with output power telemetry.
- Transmitter should count with module's temperature telemetry.

1.1.3.5 Products for Reference

Not defined until now.

1.2 Radiation Specifications

This section specifies the requirements of radiation tolerance of the parts to different species and energies based on JPL SAC-D environmental requirements document D-27906. Radiation environment consists of charged particles in high-energy solar particle events, the Earth's trapped radiation belts, and galactic rays. The model is based for a 600 km orbit with 98 degree and 90 minutes transit time. In Fig. 1.3 a representation of the orbit's satellite is depicted. When the systems should operate on 5 year missions these requirements must be followed. When the systems operate on a much shorter time term principal attention must be paid to high energy particles spectra and neutrons that could cause single event burn out. A radiation design factor (RDF) of 2 shall be used when determining the acceptability of a device for use. RDF of 3 shall be used for spot shielded devices. RDF is defined as the ratio of the part's radiation resistance and the radiation environment at the location of the part.

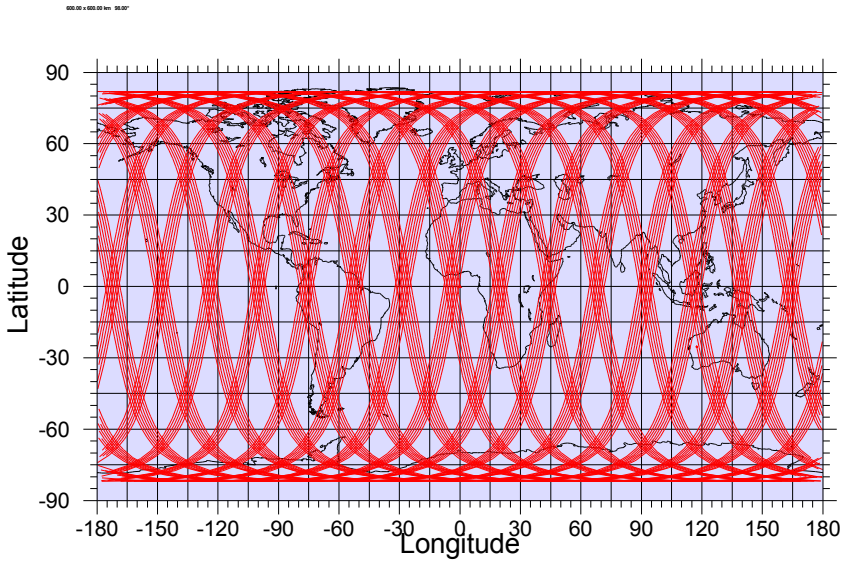


Figure 1.3: Orbits for SAC-D mission

1.2.1 Solar protons

Solar protons fluences were simulated based on a JPL91 model. The values shown in Fig. 1.5 are well in accordance with the ones on the SAC-D document and does not exceed fluences of 1.5E+11 for relevant energies.

1.2.2 Trapped protons and electrons

Trapped protons and electrons flux were simulated based with AP8 and AE8 models. The values shown in Fig. 1.5 are well in accordance with the SAC-D specs. This graphic shows that electron flux is greater than proton flux for the lowest energies but vanishes above energies of a few MeV.

1.2.3 Total ionizing dose

Total ionizing dose value is of 1.87 MRad for 1 mil shielding thickness, been trapped electrons its principal contributor. Using a RDM of 2, the selected parts should be prepared to cope with 3.74 MRad of TID.

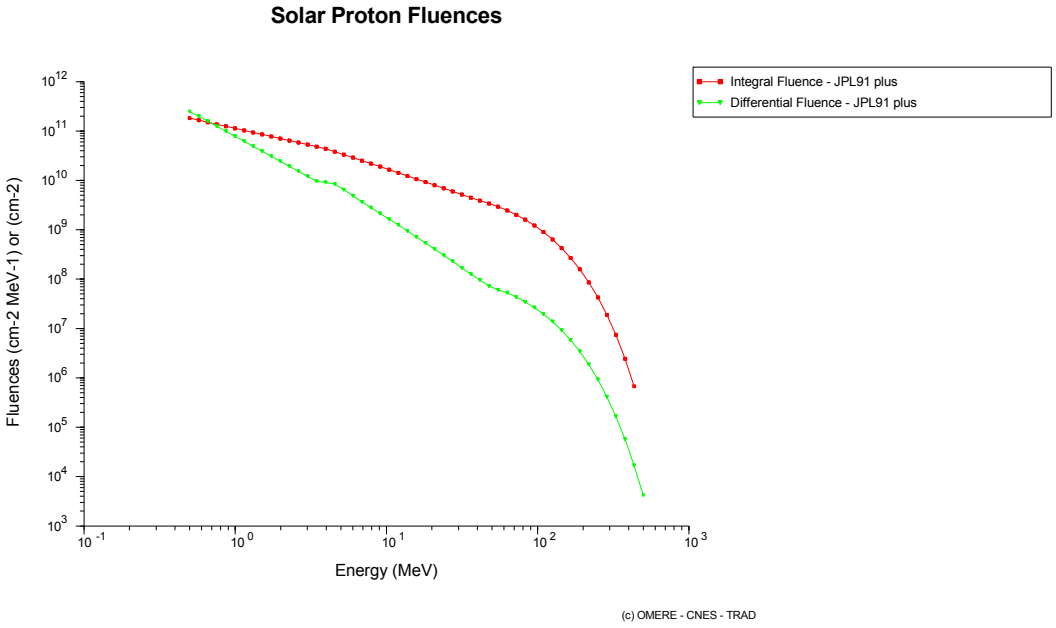


Figure 1.4: Solar proton fluences for the mission

Fortunatelly, as can be seen on Fig. 1.6 if a shielding of at least 1 mm of aluminium is used the values of radiation won't exceed a few KRads allowing parts with tolerances of tens of KRad to be used.

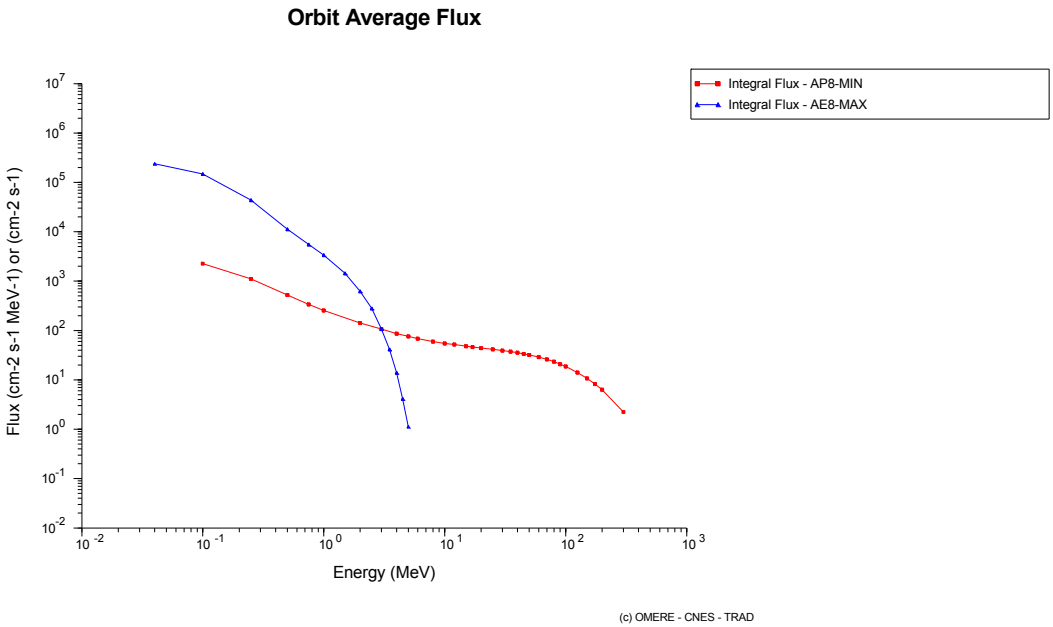


Figure 1.5: Integral proton and electron flux for the mission

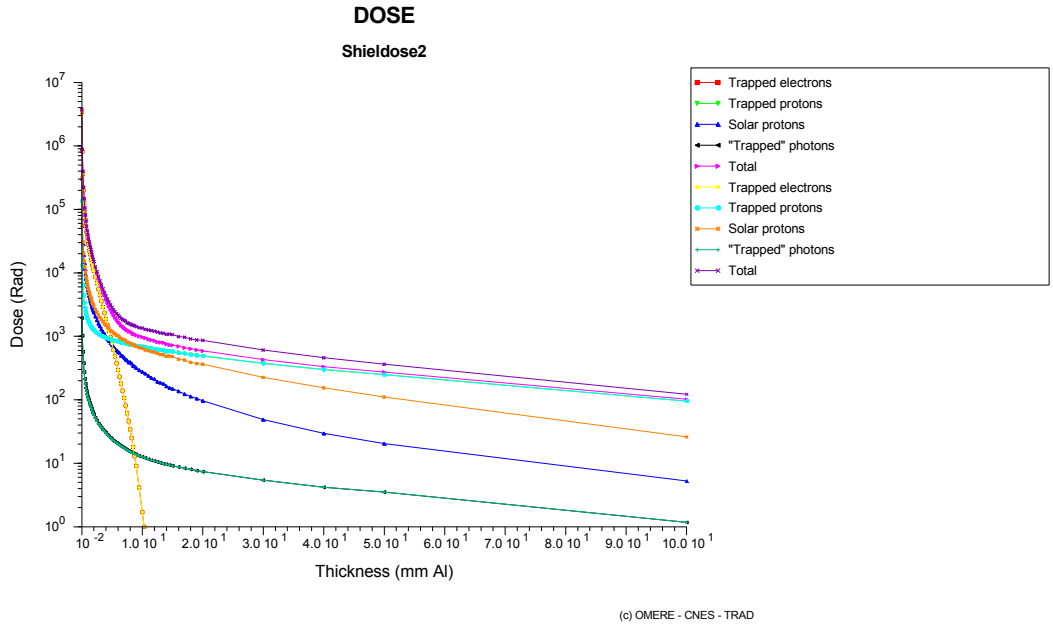


Figure 1.6: Total ionizing dose for different species as function of aluminium thickness shielding

1.2.4 Displacement damage dose

Displacement damage dose (DDD) is presented in terms of an equivalent 1MeV neutron fluence in order to facilitate comparison with test results on parts susceptible to DDD. The shield geometry is 4π steradians spherical shell of aluminum. In Fig. 1.7 and 1.8 protons and electrons fluences are shown respectively.

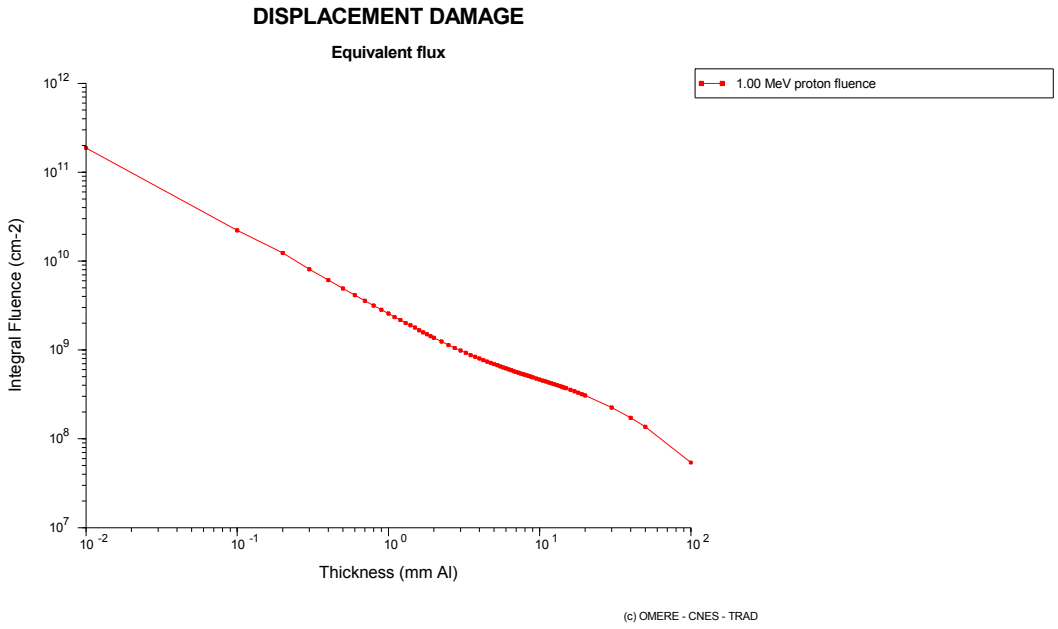


Figure 1.7: DDD equivalence to proton fluence given as function of aluminium thickness shielding

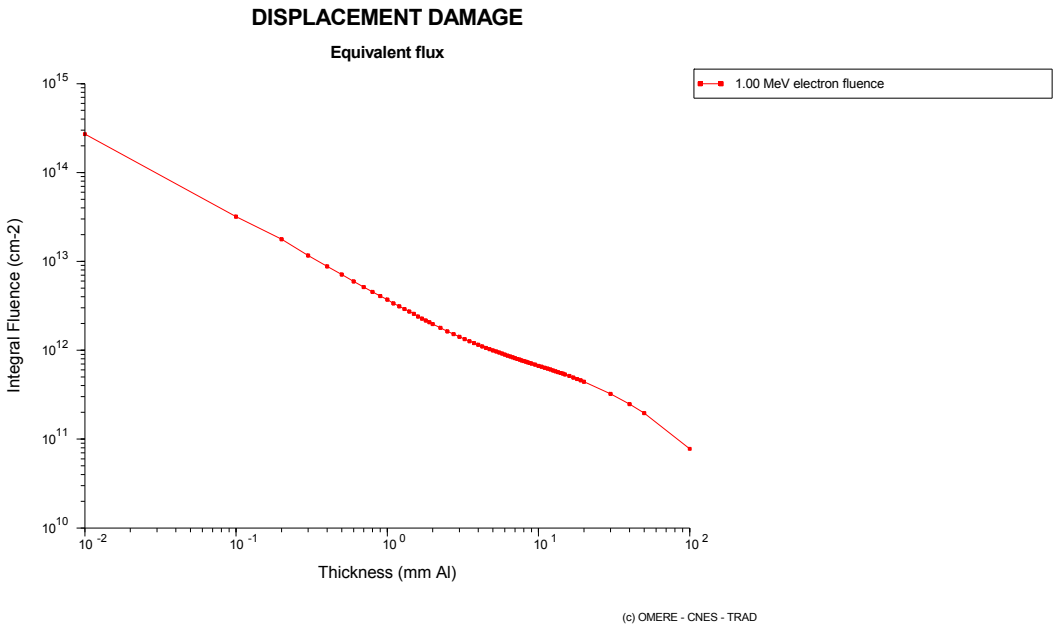


Figure 1.8: DDD equivalence to electron fluence given as function of aluminum thickness shielding

1.2.5 Single event effects

For single event phenomena evaluation, an integral linear energy transference (LET) spectrum is shown in Fig. 1.9. Simulation includes trapped protons, solar particles and cosmic rays, behind a 25 mils of spherical aluminum shielding.

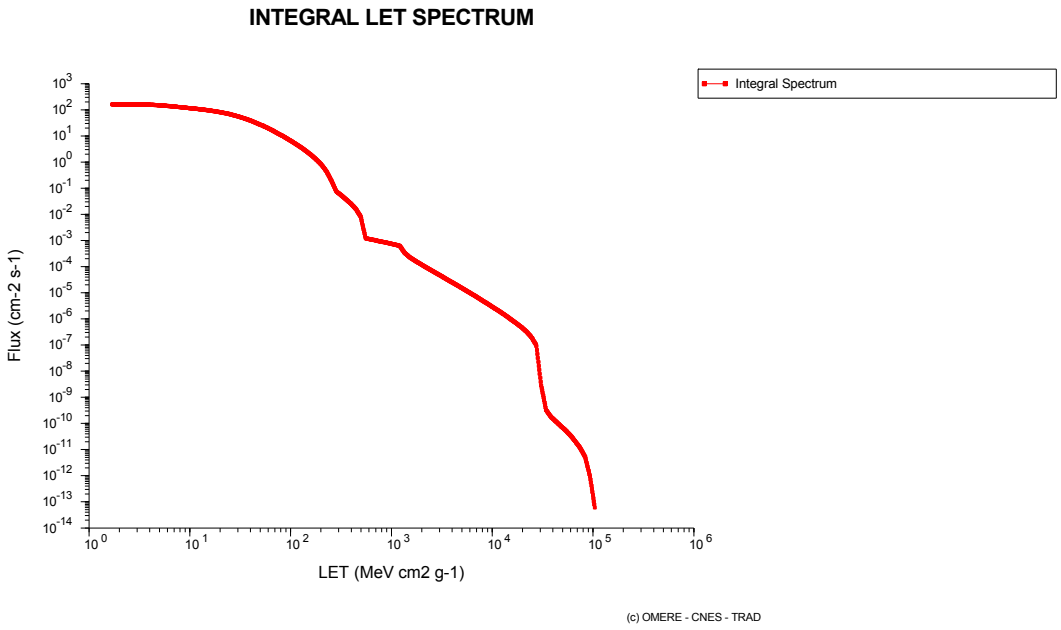


Figure 1.9: Integral LET spectrum

1.2.6 Radiation Specification Summary

All the species and energies shall be considered for design and evaluate the vulnerability of a given part. It must be noted that all calculations including the target material were performed for silicon devices and must be revised if another material is intended to be used for the construction of the devices.

1.3 Requirements Summary

Table 1.3 show an overview of power amplifier requirements in this feasibility study:

System Name	Average Power	Peak Power	Power Supply	Efficiency	Frequency Range	Modulation	Linearity	Radiation Hardening
Telemetry	10 W	10 W	28 V	≥40 %	2.2-2.4 GHz	FM	Med/High	Yes
Beacon	15 W	15 W	28 V	≥60 %	0.46-1.45 GHz	BPSK/FSK	Low	Yes
Transponder	1 W	400 W	28 V	≥50 %	5.4-9.6 GHz	Pulsed RF	Med	Yes
Data Link	10 W	10W	28 V	≥40%	8.0-8.4 GHz	TBD	Med/High	Yes

Chapter 2

Process Evaluation and Design Strategies (First Deliverable Document)

This chapter describes the evaluation aspects for foundry semiconductor processes selection and analyzes the possible strategies and methods required to design microwave power transistors and MMICs power amplifiers. The chapter is divided in two sections according to previous mentioned. In second part the subjects are treated briefly, to deepen understanding, chapters 8, 9 and 10 were added to provide background theory, equations and state of art references in the subject.

2.1 Introduction

Following with the feasibility study, must be evaluated the feasibility of each foundry process/es to accomplish with the requirements analyzed in previous chapter. The evaluation presented here is done regardless the complexity of the resulting design and no matter how much money would be needed.
To complete the above mentioned, we analyze the state of art designs alternatives and the implementation aspects involved, with the objective of establish a matrix of weighted *decision criteria*, that in turn allows to make a comparative evaluation between process according to the several trade-offs involved in the power transistor or MMIC design.

At the end of the feasibility study, the concepts analyzed and the resulting *decision criteria* developed in this chapter will be used to deliver the main conclusion, namely, a list of pre selected foundry process, discarding only whose specification clearly falls outside the specifications (e.g. the cutoff frequency is below the upper frequency limit).

2.2 Foundry Processes Evaluation (First Part)

A factor of high impact in the final design is the choice of the *Substrate Material* since the properties of this semiconductor material have the greatest influence over the final potential performance of the transistor or MMIC.
Among all the substrate characteristics, below are presented those that requires more attention:

- *Electron Mobility* and *Peak Velocity*: this properties determines in the doped semiconductor how fast the electrons in the active components can react to quickly fluctuating electric field, dictating their frequency response.
- *Energy Gap*: the energy gap in semiconductor substrate determines how high the breakdown voltage of the transistors will be, hence their power handling capability.
- *Resistivity*: The resistivity of the semiconductor substrate in its semi insulating state also has an important effect on the circuits performance. Its value determines power loss and the Q-factor of the passives components created on its surface.

Another important choice related to the semiconductor technology process is the type of *Active Device* (transistor) to be used to create an amplifier in a MMIC. Today there are many option related with this aspect, even more , in the same substrate can be realized more than one type of active devices. The most common used active devices today are the High Electron Mobility Transistor (HEMT) [39], [40] and its variants (replace the traditional FETs or MESFETs), the other is the Heterostructure Bipolar transistor (HBT) [41], [42] in all its variants, which replaces the old work horse Bipolar Junction Transistor (BJT).

Material	Electron Mobility ((cm^2/V_s))	Peak Velocity ($10^7 cm/s$)	Frequency Range (GHz)	Gain
Si	900-1100	0.3-0.7	<20	Moderate
SiGe	2000-300000	0.1-1.0	10-40	Better
SiC	500-1000	0.15-0.2	15-20	Lower
GaAs	5500-7000	1.6-2.3	>75	Higher
GaN	400-1600	1.2-2.0	20-30	Lower
InP	10000-12000	2.5-3.5	>115	Higher

Table 2.1: Characteristics of the Most Commonly Used Semiconductor Materials

Finally, aspects related with foundry services economics and support are considered.

2.2.1 Substrate Material Evaluation

The most common substrate for microwave power application is the GaAs [43], although new materials are becoming more attractive and popular today. Among others we can mention Silicon Carbide (SiC) [44] and the Gallium Nitride (GaN) [45] which was released to commercial applications one decade ago. These are both wide band-gap semiconductors, which means they have much higher breakdown voltages and an operate at higher junction temperatures.
With less power capability (up to now) the Silicon Germanium (SiGe) [42] is gaining popularity in medium power applications with cut-off frequency beyond 100GHz. More exotics substrates, such as indium phosphide (InP),are tending to take over from GaAs as frequencies extend beyond 100GHz [46]. Table 2.1 highlights the most important characteristics of semiconductor substrates related with the present feasibility study.

2.2.2 Active Device Evaluation

Once the semiconductor substrate is selected the other important aspect to be taken into account is the selection of the active device.
Two basics types of active devices are used in MMICs, field effect transistor (FET) and bipolar transistor (BJT). In turn, these devices have their own variations, for example a MESFET and HEMT transistors are variations of the original FET structure, also HBT of the traditional BJT.
Below, we present a brief description of the active devices under consideration:

- MESFET: Metal Semiconductor Field Effect transistor. Its name describe the way the metallic contact is attached to the semiconductor junction. This contact results in a Schottky contact between the gate metal and the semiconductor making a device with high frequency response and very low leakage gate contact.

- HEMT [47]: The high electron mobility transistor operates like any other FET, except the channel is constructed from a junction of two different types of semiconductor materials (known as a hetero junction) to give to the free electrons in the channel higher mobility than traditional FETs. HEMT are also referred as a hetero junction FETS (HFETs) or modulation FETs (MODFETs).

- PHEMT : Pseudomorphic HEMTs use an extremely thin layer of the different semiconductor (typically InGaAs or InGaP) which is strained to the lattice constant surrounding semiconductor, making as pseudomorphic layer; this produces a gain in electron transport properties, while the full MMIC is still being fabricated on GaAs.

- MHEMT: A metamorphic HEMT has higher mobility semiconductor layer (such as InP) grown on its surface with its own natural lattice constant.

- HBT [48]: The heterojunction bipolar transistor (HBT) is similar to the standard bipolar (BJT) except that the base-emitter junction is usually a junction of two different semiconductor materials instead of the same material with different doping. By having the emitter layer heavily doped and the base layer lightly doped, HBTs achieve the injection efficiency by the energy band-gap difference at the junction, which prevents holes form being injected into the emitter. This allow the base layer to be more heavily doped which greatly reduces the base resistance, and this reduces the transit time of the device and increases its frequency response.

To conclude we present Figure 2.1 to show how substrates technology and active devices interrelates. This figure is a rough view of the current state of art of microwave semiconductors substrates and possible active devices. In this figure is easy to observe the power-frequency relationships and the limits for any of them for each semiconductor material and also, what kind of active device is available in each substrate.

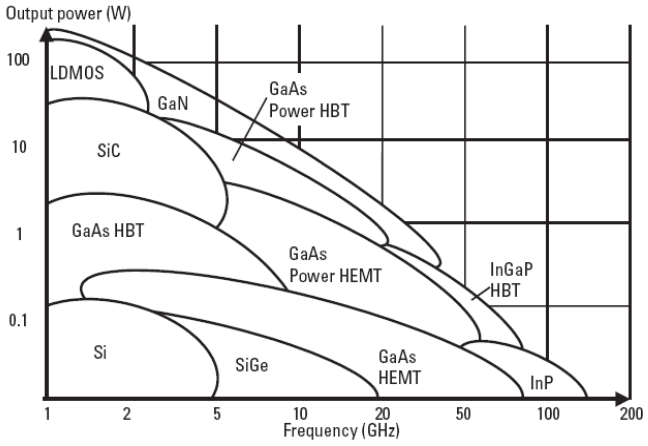


Figure 2.1: Output Power versus Frequency for Various Transistor Technologies

2.2.3 Foundry services

Finally, we must consider what procedures the designers may go trough when designing a MMIC with an external foundry.
Interaction with foundry starts with discussions on a informal basis between the customer and foundry engineers regarding the foundry capability and available options. This will be on a very general level, discussing aspects such as the process technology available, key performance benchmarks of the active devices on the process, and examples of the type of circuits that have already been produced by the foundry. This is also the time when customer should ensure that the foundry can supply the electronic design data that can be used with CAD simulation tools (process design kits, PDKs).
When arrived to a conclusion that the foundry process can be useful in the project a Mutual Non Disclosure Agreement bust be singed between foundry an PDKs user. This will allow to foundry to pass much more and detailed information.
After the design has been completed, on PDKs basis and foundry support, it must be fabricated. For that purpose the customer must sign a wafer agreement with the foundry.

Figure 2.2 shows the basic step in designing and fabricating a MMIC together a foundry service.

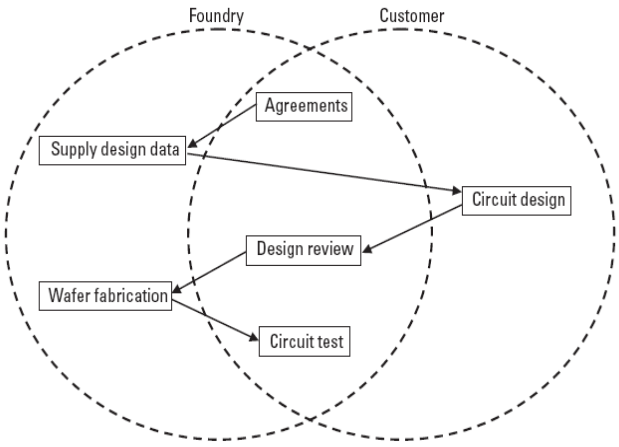


Figure 2.2: Steps for Designing and Fabricating and MMIC using a Foundry

2.3 Design Strategy and Methodology (Second Part)

The design strategy is be divided in three parts that can vary according to the EDA design tool that can handle the foundry models. Thus, the design strategy is be divide as follow:

- *Architecture Design*: At this step must be calculated: The device size and number of active devices in parallel (if needed) for a specific power at certain operating frequency. If the paralleling is not enough to achieve the output power requirement, power combining structures must be analyzed.
- *Small Signal Design*: Small-signal design is the fast and simple way of designing the matching and biasing networks to achieve the basic bandwidth, gain, and input match. Small signal design is mainly related with the calculation of input and output matching networks and after that the verifying of stability aspects.
- *Large Signal Design and Optimization*: Large-signal design is the optimization of the output matching circuit for the best performance (output power) under large signal operating conditions. This involves tweaking the output matching circuit using the minimum amount possible of time consuming nonlinear analysis to take account of the nonlinearities encountered at the extreme ends of the load line.

In the following, a more detailed description of the design strategies and methodologies described above:

2.3.1 Architecture Design

The architecture of the transistor or PA MMIC should be decided based on the requirements.
The choice of the architecture involves deciding which MMIC process to use, what size of unit cell device, how much gain provides the active device, and what power splitter and combiner techniques should be used (if needed).
Typical requirement specification for a power transistor or PA:

- Frequency Bandwidth & Frequency Carries
- Transmission Gain (S_{21})
- Output Power at 1-dB Gain Compression Point (P_{1dB})
- Saturated Output Power (P_{SAT}, usually reached between P_{2dB} and P_{3dB})
- Power Added Efficiency (PAE), defined as $(P_{OUT} - P_{IN})/P_{DC}$
- Linearity (expressed as a third-order intercept point referred to the output: P_{TOI})
- Operating Temperature Range

2.3.2 Selection of Power Semiconductor Process

The choice of the Transistor or MMIC process is primarily determined by the operating frequency and efficiency required. Below 10GHz, MESFET and HBT are commonly used, with HBTs typically being the more efficient. At a higher microwave and millimeter wave (Above 10GHz), high electron-mobility transistor (HEMT) processes are usually required.
For each technology, it is possible to have a process optimized for power applications, so this may also influence the choice of process. These power processes are generally defined in terms of watts of output power per unit size of the active device. For MESFET and HEMT devices, the current flows under the gate and is scaled up by increasing the *width of the gate*, so these processes are defined in terms of the output power per millimeter width of the device gate (W/mm). On th eother hand, in HBT devices the current flows down through the emitter contact and is scaled by increasing the *length of the emitter*, so these processes are defined in terms of the output power per millimeter length of the device emitter (W/mm). Foundries may quote the output power per millimeter length or width of a process in terms of the saturated or $1 - dB$ compression output power of a device and at a Class A or B bias point.
Once the process is selected, the output power specification defines the size of the required device (total width of the gate in millimeters for HEMT and MESFET and total length of the emitter in millimeters for HBT). For example, if a 5 Watt output power PA is designed on a 1W/mm HEMT process it would require at least 5 mm of the total gate width in the output stage.

2.3.3 Considerations on Optimum Unit Device Size

Once the total size of the power device required for certain output power is calculated, the question becomes whether we can have just one device of this size or if we need to use several smaller devices. To decide this, we need to look at the general rules applying to scaling of MMIC's active device, namely:

- *First, as the device size increases, the output power increases*
- *Second, as the device size increases, the gain decreases*

To understand the trade-off between these effects, we need to look more closely at the basic device characteristic and how they scale with increasing device size.
The output power P_{out} is proportional to the device size because it is a function of the drain voltage V_{drain}, the drain current I_{drain}, and the efficiency η. The drain voltage is limited by the breakdown voltage, which is itself a function of the substrate material and the device layout and is fixed for each process. The drain current is a function of the device structure, channel doping density, and so forth, and is proportional to the width of the gate. The efficiency is a function of the device type (HBT or HEMT) and is fixed for each particular process. Therefore, the output power is a constant multiplied by the total width of the device, as showed below:

$$P_{out} = \eta V_{drain} I_{drain} = k.gate_{width} \tag{2.1}$$

Conversely, the device gain is inversely proportional to the device size because the increased parasitics associated with the larger device degrade the device gain. These large FET parasitics include the gate source capacitance, the source inductance, the phase errors along the gate, the phase errors between the gate fingers, and the thermal effects.
Then, to avoid the loss o gain, large power FETs are constructed by increasing the width of the individual gate fingers and using multiple gate fingers as showed in figure 2.3.

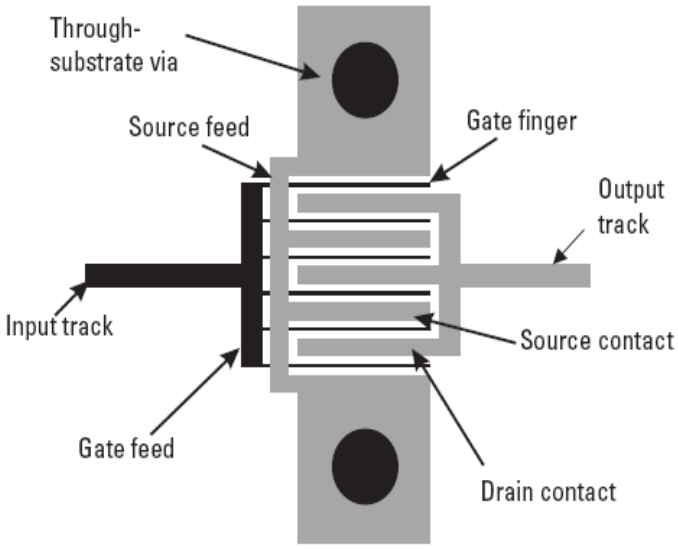


Figure 2.3: Schematic Diagram of a Large Power FET Device

Below, we review the main physical aspect of the active device and their relationship with the device size:

- *Capacitance.* The gate-source capacitance is the capacitance between the gate feed and the source feed metalization and increases with the numbers of gate fingers being fed. This increased capacitance lowers the input impedance of the device and causes the device gain roll-off more quickly with frequency.

- *Inductance* The source inductance is the inductance produced by the current path from all the channels along source feed metal down through the substrate bias to the back-ace ground plane. As the number of gate fingers increases, the increasing distance between the central gate fingers and the source bias at the side of the device produces significantly more inductance.

The inductance in the source path of a transistor has the effect of producing negative feedback and directly reduces the transistor gain.

- *Phase Errors*: Phase errors along individual gate fingers are produced when their dimensions approach a significant fraction of wavelength of the signal traveling down them. When this happens, the current flowing under the gate near the gate feed meta may be slightly out of phase with the current flowing under the far end of the gate. If the currents from all the devices gate do not add up in phase, the effective transconductance is reduced and he device gain is decreased.
  Other phase errors are related to those that arise when the device size's become large. In this situation the distance between the input signal track and the central gate fingers is different from that between the distance to the outer gate fingers.

- *Thermal Effects*: The transconductance is an inverse function of the channel temperature. Each transistor produces heat because the DC bias power applied to the device is not completely converted to RF output power. The heat produced raises the temperature of the channel until the equilibrium is reached with the surrounding environment.
  As a rule of thumb, taking into account the mentioned above, at frequencies below 1 GHz, the phase errors become insignificant, and only the thermal effects need to be considered. At these frequencies, two or more smaller transistors could be used instead of one large device fr thermal management purposes. At higher frequencies, between 1 GHz and 30 GHz, the parasitic effects and phase errors are significant and will influence the design together thermal effects. Above 30GHz only phase errors must be considered.
  For all the mentioned before, the optimum device is the one that gives the maximum amount of power and still has usable signal gain over the specified frequency range. A goo rule of thumb is to select the largest device that still exhibits a G_{MAX} of $10dB$ at the high end of the specified frequency range.
  The selected unit device size has a known and fixed output power level, so if the specification requires more power than one unit device can provide. more than one unit device must be used in parallel in the output stage. In this case power splitters and combiners must be used.

2.3.4 Number of Amplification Stages

As mentioned in previous paragraph the typical power gain of a single stage is around $10dB$, which certainly produces a reasonable power added efficiency (PAE). For this study was not specified the PAE requirement (in space applications is critical). However, the effect of a single stage's power gain is reviewed and considered as another important design criteria helpful to analyze the semiconductor process and device selection.
The PAE is a measure of how efficiently the design converts the DC bias power into additional power at the RF frequency. The definition of PAE is given by 2.2:

$$\text{Power Added Efficiency (PAE)} = (P_{out} - P_{Pin})/P_{dc} \tag{2.2}$$

where P_{in} is the RF power of input, P_{out} is the RF power output and P_{dc} is the power delivered by dc power supply.
The RF output power is the RF input power multiplied by a constant called power gain G:

$$P_{out} = G.P_{in} \tag{2.3}$$

thus, equation 2.2 can be re written as follow:

$$PAE = \left(P_{out} - P_{out}/G\right)/P_{dc} \tag{2.4}$$

which indicates that when stage gain tends to infinite, P_{in} tends to 0, and the PAE reduces to simply the output RF power divided by the DC bias power as shown next:

$$PAE = P_{out}/P_{dc} \tag{2.5}$$

the expression 2.5 is referred over the *drain efficiency* definition since describe more precisely the device efficiency. In turn, the efficiency depends of the process technology and the type of active device. *Drain Efficiency* is used along this feasibility study due to its importance in power and thermal calculations.

2.3.5 Active Device Paralleling

Parallel devices are simply two or more devices connected up in parallel by transmission lines. This approach is only really useful at low RF frequencies (¡ 1 GHz), where the phase difference between the device feeds is a sufficiently small fraction of the transmission line wavelength. This technique is mainly applied in order to separate devices physically for better thermal management within the power transistor or MMIC. The main disadvantage of this approach is that the resulting impedance at the common node is very low and hard to match over a broad frequency range.

2.3.6 Active Deices in Connected in Series

Another way to increase the output power than paralleling devices is to arrange them in series configuration. In this form the rupture voltage of an active device is increased by N (where N is the number of series devices). By increasing the maximum output voltage increases the output power since, for the same current a higher output voltage is allowed.
The series configuration is not the most recommended way to increase the output power due to the fact that the input and output impedances decreases by N. It is considered as a secondary option in this feasibility study. Shall be evaluated only when the technology process have a low breakdown voltage. In Chapter 9 the details of this technique are discussed.

2.3.7 Power Splitting and Combining

When the RF power delivered from a single active device not fulfills the power specification, the main option is to parallel single devices to add up its individual output power. In RF this summation is done with power splitting and combining structures.
There are numerous techniques that are currently used on, or could be applied to carry on a power combining of power devices or power amplifiers. These techniques are quite similar either they are implemented outside the chip die (Hibryd or MICs [49]) or inside the chip die (MMICs [24]). The present feasibility study deal with both options in order to obtain the designs trade-offs to provide a selection criteria. The integrated option is a priori preferred due to reliability and size aspects.Only passive splitters and combiners are covered is this study.
The most important attributes of all these types of combiners that must be take into account are:

- *Insertion Loss.*
- *Physical Size.*
- *Frequency Bandwidth.*
- *Bias Compatibility.*
- *Effect on Odd-Mode Stability.*
- *Equal Phase Split.*

The *insertion loss* in the combiner is particularly important after the last gain stage (if several stages were used), and must be minimized to obtain a good power added efficiency. Also the size in this combiner is critical.

A more detailed study of power combining and power paralleling techniques including the benefits and drawbacks related to the size, insertion loss and stability is presented in Chapter *Combining*.

2.3.8 Aspects related to the Active Device Temperature

Since any active device has a finite efficiency (less than 100%) not all DC power that incomes to the device is converted into RF power. Thus, the DC power not converted to RF power is dissipated in the active device as a heat. Due to the finite thermal impedance of the active device, the heat generation raises the device's temperature above ambient temperature up to certain equilibrium point.
Active device parameters are functions of their temperature; moderate increases in temperature decrease device gain an power, and large increases in temperature compromise the device's reliability. For that reasons, the temperature of the active devices must be managed carefully. To achieve this goal is very important to get the processes (substrate) thermal conductivity and thermal resistance value which in turns should be calculated according the transistor structure (see in Chapter Thermal, Multi-finger

thermal model). Whit the thermal resistance value and the processes maximum operating temperature, according to certain life cycle criteria, one can calculate the maximum dissipated power by the active device. This value must be complemented whit the maximum output power obtained with the 10dB gain criteria.
The criteria are:

- Power transistors have a maximum allowed operating channel temperature.
- The channel temperature should be minimized to extend the life cycle.

2.3.9 Impedance Matching

Input- Output impedance transformation (matching networks) are an essential part of a power amplifier design. In power amplifiers, impedance matching is crucial to achieve the better possible transference from device output to the load. When better the matching better the PAE. This feasibility study will consider among the available techniques to find the optimum matching circuit in terms of: insertion loss, matching loss, allowed VSWR, matching circuit size and implementation complexity. Of course, frequency and bandwidth are also considered, but the previous mentioned are those aspects that have influence great on reliability aspects. Thus, insertion loss is related with PAE and therefore with thermal behavior and, matching loss is related with VSWR and therefor with maximum allowable output operating voltage.
There are a variety of matching network techniques, see for example [50], but from present work perspective we classify the matching networks into two main categories which are independent of the matching technique. These categories are: *Matching Networks with Lumped Components [51]* and *Matching Networks with Transmission Line Components [52].*
Both ways to implement the matching circuitry have their own advantages and disadvantages and are highly dependent of the semiconductor process technology.
Chapter 10 presents the main aspects of the subject together the feasibility hints and decision criteria. Also a brief background theory on matching networks is included to enhance the decision making process.

2.4 Device and Circuit Design Flow

The design flow shall follows the sate of art criteria mainly based on design criteria and steps dictated by each foundry. Even each foundry have its own design flow, all of them are quite similar. In all cases the design flow relies on the EDA tools and are highly dependent of the simulation models available for active and passive devices provided by the foundry (PDKs). Thus, to succeed in the design task, highly confident models must be provided by the foundry.
Basic design flow is as follows: DC Analysis for selected bias (Class AB or C in case of pulsed), S Parameters Analysis, Harmonic Balance for large signal adaptation [27] and electromagnetic simulation

optimization.

After the analytic design the circuit must be placed or mapped to a layout design, namely, it is necessary to convert the physical models into a physical component in the semiconductor substrate. This mapping is ruled by foundry design rules (DRC process). Some foundry provides on-line DRC verification, this feature is pretty welcomed since this tool option allow to the designer work with the up to date DRC rules, thus is warranted that the design to the foundry is highly confident.

Figure 2.4 shows a typical flow diagram for MMIC design:

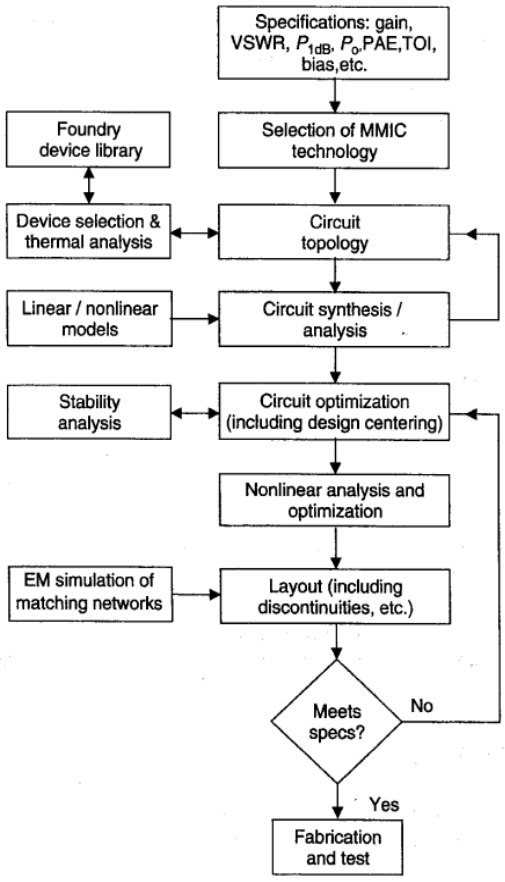


Figure 2.4: Flowchart for an MMIC power amplifier design

2.5 EDA Tools Provided By Foundries

2.5.1 Simulations Tools

Simulation tools are one of the most important design tool together the foundry process handbook and design rules. We expect that foundries provide process design kits that allow to work with simulation tools like: DC Analysis, S parameters (Matching Network and stability), Harmonic Balance (Load Pull

Output Matching Network Optimization) and if possible 2D/3D electro magnetic Simulator (Matching Network Optimization).
LAPSyC and GISEE laboratories have the capability to work with Agilent ADS and Cadence Virtuoso EDA tool, even more, Goldengate software (ADS feature) allows to use together Cadence and ADS the take out the best feature of each one.
In advance we present a list of EDA simulation software provided by foundries under investigation 9.1, the list shows only the software compatibility, the simulation tools that each PDK offers can vary from process to process (even for a same foundry).

Triquint Processes	ADS Win	ADS Linux	Cadence	EM	GoldenGate
TQP15	yes		yes	yes	yes
TQHBT3	yes		yes	yes	yes
.25um Xku pHEMT 3MI	yes		yes	yes	yes
.25um GaN on SiC 3MI	yes		yes	yes	yes
UMS Processes					
PPH25X	yes				
HB20P	yes				
WIN Processes					
HO2U-02	yes		yes		yes
HO2U-32	yes		yes		yes
HO2U-43	yes		yes		yes
PP50-11	yes		yes		yes
Cree Process					
Gan HEMT MMIC	yes				
RFMD					
FD30	yes		yes		yes
GaN 1	yes		yes		yes
GaN 2	yes		yes		yes
GaN 3	yes		yes		yes
IHP					
SG25H3		yes			
SGB25V		yes			
SG13S		yes			
TowerJazz					
.13 nm SBL13	yes		yes		

Table 2.2: Foundries EDA Tools

2.5.2 Large Signal Models

Large signal model is one of the most useful tool that a foundry company can provide to design high power actives and passives. Moreover, without this model, only small signal design can be done, so the design is restricted to make design optimization by trial and error with laboratory measurements which is time consuming and costly. For that reason the selection of the foundry process will be strongly affected by the type of large signal models offered. In next Chapters 5 and 6 we will discuss the details about models and EDA tools.

2.5.2.1 Thermal Models

Thermal model means here a large signal model that include the effects of thermal device behavior. It is highly desirable that the large signal model provided by foundry's PDKs include the thermal behavior of the active and also passive devices. As mentioned before the selection of the appropriate model will impact strongly in the design results. Minimizing the number of steps from simulator design to manufactured device.

2.6 General Summary

As a concluding remarks we can mention:

- The choice of the substrate go first and defines conditions the overall performance.
- The choice of the active device go in second place since depend on the substrate selection.
- For the foundry selection is crucial the offered simulation models and available EDA tool.
- The design aspects to consider are: architecture, active device size, temperature and impedance matching.
- The overall design flow is conditioned by the simulation models.
- The decision criteria developed here will be completed with the information resulted from chapters 3, 4, 5 and 6 to later deliver the feasibility study conclusions in chapter 7.

Chapter 3

State of Art of Semiconductor Devices and Technology (Second Deliverable Document)

This chapter gives an overview on the current state of art of the microwave semiconductor technologies (devices and substrates) for monolithic integrated circuits (MMICs) manufacturing. Si, SiC, GaAs, GaN and InP substrates and devices are compared in light of different performances with emphasis on maximum output power and efficiency. Both, academic and industry data are included. The devices under study are those intended to be used in microwave power applications up to frequencies defined by the IEEE X band (8GHz-12GHz maximum). To better understating of the subject, historical milestones are included. The chapter is divided as follows: First the semiconductor substrates characteristics are reviewed, after that, a survey of current active devices is presented. Since each active device can be implemented in more than one type of substrate, the same device will be presented repeatedly if necessary to highlight the differences. In turn, examples of research and commercial MMICs are included.

3.1 Introduction

Active devices are mainly divided in two major groups: *Bipolar* Junction Transistor (BJT) and *Unipolar* Field Effect Transistor (FET). Nowadays, the BJT and FET acronyms are almost no longer used in microwave applications since the active devices described by them were replaced with more sophisticated versions. Thus for example, BJT [53] was replaced by HBT [42]. The new acronym stands for Heterostructure Bipolar Transistor which means that the base emitter junction is no longer manufactured by the junction of two layers of same semiconductor with different doping profile. Instead of that, the new junction is build with two or more layers of different semiconductor materials. This is the reason why these devices are called heterojunction transistors or also heterostructure transistors.
On the other hand, the acronym FET [53] was replaced by HEMT [45] that means High Electron Mobility Transistor. This new device is build replacing the traditional FET channel with a new one manufactured with two ore more layers of different semiconductors. Roughly speaking this new channel structure decreases the scatter of flowing electrons thus, decreases the heat and accelerates its transport velocity (among others favorable characteristics).
The mentioned devices are not the only ones. There are perhaps other types of HEMTs devices like pHEMT and mHEMT, that means respectively pseudomorphic HEMT and metamorphic HEMT. The words pseudomorphic and metamorphic describes how the different layers (crystal structures) are joined one to each other. From the device point of view, there are not differences between HEMT [54], pHEMT [54] and mHEMT [54] being in essence all the same active device. The differences arises in the field of performance metrics like output power, noise figure, linearity, etc.
Respect to FETs devices, nowadays were replaced (in the microwave arena) by MESFETs [55] or MOSFETs , [56], [57]. The acronym for the first describes how the gate contact is done directly trough a metallic contact, from there derive its name, Metal Semiconductor Field Effect Transistor. The second acronym stands for Metal Oxide Semiconductor Field Effect Transistor. In this device the gate contact is made off trough a semiconductor oxide layer [57].
The most of the above mentioned devices, either bipolar or unipolar, can be found manufactured on different types of semiconductor substrate. For example, a device named InGaP/GaAs HBT means a HBT active device manufactured on GaAs substrate with its base build with layers of Indium (In), Gallium (Ga) and Phospide (P). Due to many existent combinations of *active devices-substrates-terminal layers* we proceed to ordering the information in the following manner. First, the next section describes the most common semiconductor substrates used to manufacture microwave discrete and MMICs devices. After that, we group the active devices in two sub groups as mentioned before: unipolar and bipolar. Thus, each device is classified according to the substrate and layer material configurations.
The information in this report was derived from the following combinations of sources:

- Extensive literature and Internet research.
- Manufacturer's product literature.
- Technical articles and research publications.
- Conference proceedings.

- Press Releases and other promotional material.

From now on, the active devices under review will be mostly those related to microwave power applications.

3.2 Semiconductor Substrates

The substrate is a solid semiconductor substance (usually planar) onto which a layer of another semiconductor, insulator or conductor substances is applied to obtain certain device or circuit properties. The term generally refers to a thin slice of material such as silicon, silicon dioxide, sapphire, germanium, gallium arsenide, etc. The slice serves as the foundation upon which electronic devices, i.e. integrated circuits, are deposited.
Next, we will roughly describe the semiconductor substrates that have potential capability and characteristics for the applications involved in this feasibility study.

3.2.1 Silicon Substrate(Si)

Silicon is an elemental semiconductor material because of four valence shell electrons. It occurs in nature as silica and is refined and purified to make wafers. Pure silicon is intrinsic silicon. The silicon atoms bond together in covalent bonds, which defines many of siliconś properties. Silicon atoms bond together in set, repeatable patterns, referred to as a crystal. Germanium was the first semiconductor material used to make chips, but it was soon replaced by silicon. The reasons for this change are:

- Abundance of silicon.
- Higher melting temperature for wider processing range.
- Wide temperature range during semiconductor usage.
- Natural growth of silicon dioxide.

One of the most important features of the Silicon relies in its Oxide. Silicon dioxide (SiO2) is a high quality, stable electrical insulator material that also serves as a good chemical barrier to protect silicon from external contaminants. The ability to grow stable, thin SiO2 is fundamental to the fabrication of Metal-Oxide- Semiconductor (MOS) devices.
For power RF and microwave devices a non desirable property, is its semiconduction property which in turn means high substrate losses. In any case, novel devices are manufactured on this substrate that achieved impressive operating frequencies and power as we will discussed later.

3.2.2 Silicon Carbide Substrate (SiC)

Silicon Carbide is made up of equal parts of Silicon and Carbon. Both are period IV elements, so they will prefer a covalent bonding. Also, each Carbon atom is surrounded by four Silicon atoms, and vice versa. This will lead to a highly ordered configuration, which means a single crystal structure. The latter implies that a stable stacking of atoms can be done through a large sample of semiconductor material. Exist several configurations of atoms stacking. They are called: 3C, 2H, 4H and 6H [55]. Of these, 4H and 6H are of interest for substrate making since large wafers can be designed.
Silicon Carbide substrate is commonly used for high power transistor (mainly MESFET [55]) or a as substrate support for GaN devices or MMICs.
The main features of SiCs substrates are: low on resistance, wide bandgap, high power and high temperature. Table 3.1 shows a comparison of substrate properties. The main advantage , which highly differ from other substrates, is its high field breakdown voltage. Active devices made on SiC substrates has the highest possible breakdown voltage [58]. In opposition, its cutoff frequency is commonly below the X band applications (see Figure 3.1). Thus, for high frequency applications is customary to found a SiC substrate as a support substrate of Gallium Nitride devices.

3.2.3 Gallium Arsenide Substrate (GaAs)

Gallium Arsenide is a compound of the elements Gallium and Arsenic. It is a III-V semiconductor, and is used in the manufacture of devices such as MMICs, LEDs and solar cells among others.
One of the principal attraction for use of GaAs is its characteristic semi-insulating (SI) property. This means that very high frequency circuits can be fabricated from GaAs. In contrast, it is much more problematic than conventional silicon, since has a much higher resistivity, i.e. it is a semi-conductor.
A detailed analysis shows that GaAs provides benefits from its electron-dynamics properties. In equivalently doped n-type GaAs and Silicon, the effective mass of the electric charge carriers in GaAs is fair less than silicon. This means that the electrons are accelerated faster than in silicon.
The main features of the substrate are depicted in table 3.1.

In the past five ten years many of the technological difficulties that characterize GaAs,for example the fragility, have been overcome. Today, the industry is on the threshold of a new era of mass production capability. That threshold arise from the commercial availability of much larger, i.e. 6-inch (150mm) diameter GaAs substrates.
GaAs substrates for active GaAs devices have been used in satellite and military application since 1990s as a main enabler of microwave technology [43] . Today devices manufactured with GaAs are facing the challenges of others competitors, either in power or frequency aspects, but GaAs reliability characteristic are still a major advantage in space applications [59].
The industry of GaAs devices is in its mature age with several manufacturers around the world like: Triquint, Win Semiconductor, OMMIC, UMS, GCS, RFMD, BAE systems, Knowledge On, among

others, although the mentioned cover almost the 100 % of GaAs market.

3.2.4 Gallium Nitride Substrate (GaN)

Gallium Nitride is a compound of Gallium and Nitride. It is a binary III-V direct bandgap semiconductor used in bright light emitting diodes since 1990s. The compound is a very hard material that has a Wurtzite crystal structure. Its high bandgap of 3.4 eV has special properties for applications in high power high frequency devices. Its sensitivity to radiation is low, making it suitable for solar cells for satellites.

In contrast to other semiconductor devices, GaN based devices are exclusively prepared by hetero epitaxy onto foreign substrate materials [60] and [61]. Compared to well established semiconductor materials such as Si, SiGe or GaAs, some of the more challenging aspects of GaN based thin film technology come from the fact that the substrate material used today (i.e. sapphire, Si, GaAs, $LiGaO_2$, AlN or SiC) have very different properties than device layer itself.

However, it is now widely accepted that the ultimately possible performance on GaN based devices can only be reached by the use of the homo epitaxy onto bulk GaN or AlN. Unfortunately, despite many years of intense research, the production grade size and quality for power applications are not feasible (GaN substrates are slowly entering in production in Japan for blue led applications [62]).

For these reasons, GaN substrates can not founded as a stand alone materials for power applications. Instead, the manufactures sells GaN devices or technology process supported by other semiconductor materials. For example, Triquint, Northrop Grumman, Cree and BAE manufacture GaN on SiC, in opposition Nitronex sells GaN devices grown on Si substrate. Supporters of Si on GaN combination claims based on the lower cost and integration capability with optoelectronics [63] but the insertion of the Si based substrates for GaN into the power application mainstream is still an open issue.

Table 3.1 shows the main characteristics of GaN.

3.2.5 Indium Phosphide Substrate (InP)

Indium Phosphide is a binary semiconductor composed of Indium and Phosphorus. It has a crystal structure identical to GaAs and most of the III-V semiconductors.

InP is used for high power and high frequency electronics because its superior electron velocity compared with other compound semiconductors.

Unfortunately, InP substrates are much more expensive compared to GaAs substrates. InP substrates are only available in small diameters (4-inches), which makes it hard to compete with the cost per chip of GaAs transistors fabricated on six inch wafers.

Today InP based devices are achieving an impressive performance in terms of noise figure and cut off frequency although the power capability should be addressed very carefully in contrast with other technologies [54].

Companies like BAE, Northrop Grumman, Triquint, GCS, Win Semi and OMMIC, among others, have

in their product portfolio InP based device products.

Next, we present one figure and two tables intended to give a pictorial description of the possibilities of active devices and substrates combinations with the applications in mind.

Figure 3.1 shows the relation between the substrates and their power and frequency capabilities.

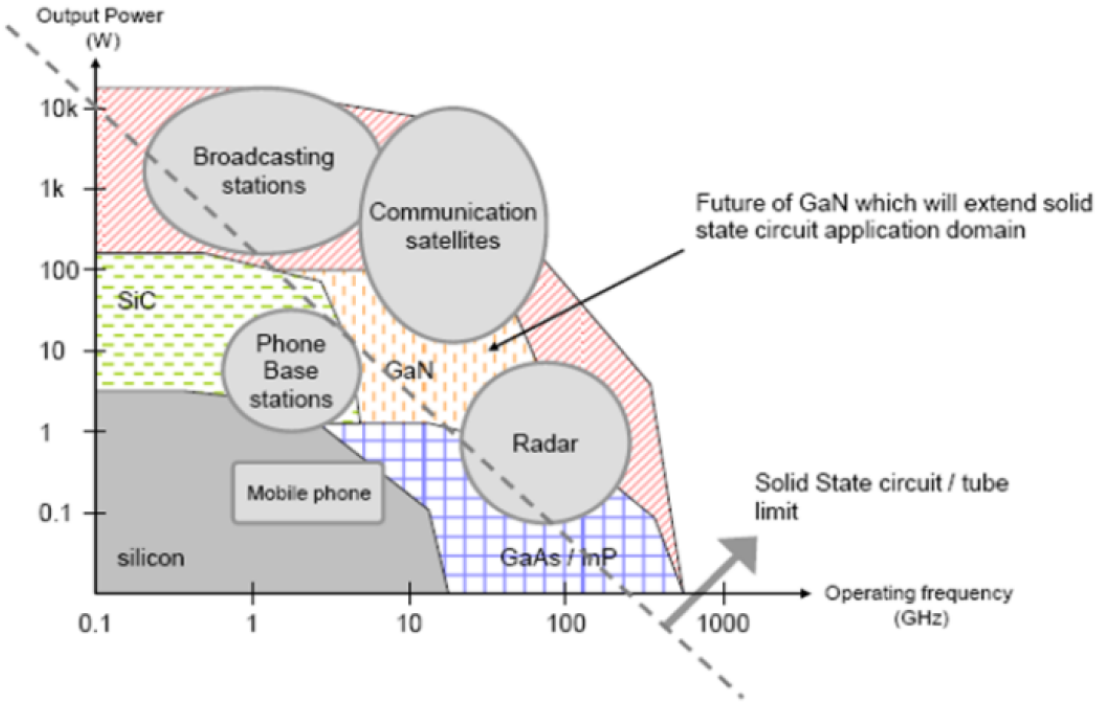


Figure 3.1: Technology versus Power and Frequency of Applications

Table 3.1 describes the main substrates characteristics related to power and frequency aspects and which active devices are possible in them. Also it is shown shows the best featured applications for each substrate.

MMIC Substrate	Electron Mobility	ϵ_r	RF Loss	Thermal Resistance	Active Device	Application
GaAs	$0.85m^2/V/s$	12.9	Low	$46W/\circ C/m$	MESFET, HEMT, pHEMT, HBT, mHEMT	PA, LNA, Mixers, Attenuators,Switches, etc.
Si	$0.14m^2/V/s$	11.7	High	$145W/\circ C/m$	LDMOS,RF CMOS,SiGe HBT	Mature for low power mixed sginal Applications
Sic	$0.05m^2/V/s$	10.0	Low	$430W/\circ C/m$	MESFET	Very High Power below 5GHz
InP	$0.60m^2/V/s$	14.0	Low	$68W/\circ C/m$	MESFET, HEMT	mm-wave
GaN	$0.08m^2/V/s$	8.90	Low	$130W/\circ C/m$	HEMT	High Power

Table 3.1: Semiconductor Substrates for MMICs

Next table (3.2) shows the current state of art of *recommended use* for active devices and substrates technologies combination, at certain power and frequency of application. This table gives to the reader an almost complete overview of the available devices and technologies. It is not a closed recipe that must be followed strictly. Instead, serves a as rough guidance of the technological possibilities at current date. In next Sections this subject is treated more deeply.

Application	Frequency	Device Process
Low Noise Amplifier	1-10GHz	GaAs MESFET
	10-100GHz	GaAs pHEMT
	>100GHz	InP
Medium Power (<10W)	1-10GHz	GaAs HBT, GaAs MESFET
	10-100GHz	pHEMT
High Power (>10W)	1-10GHz	GaAs MESFET, GaN HEMT, SiC HEMT
	10-30GHz	GaN
Switches for Digital attenuators and phase shifters	0.1-20GHz	MESFET
	20-100GHz	pHEMT
Low power mixed signal	1-80GHz	SiGe BiCMOS
VCO	1-100GHz	GaAs HBT

Table 3.2: MMIC Recommended Process State of Art (From [64])

CONCLUSIONS: In this section we presented a brief description of the main substrates commercially available. In turn, these substrates could deliver the power and frequency requirements needed in the applications and products that this feasibility study is pursuing.
A detailed state of art of devices and MMICs manufactured on such substrates is considered below.

3.3 Active Devices

In this section we present a detailed study of the active devices useful as discrete devices for microwave power amplifier application or for MMICs power amplifier integration up to X band frequencies. Although for the current study, a review of X band device 's performance is enough, results related to Ku or K bands (or even above) will be included accordingly (when necessary or useful) since most of the novel results have been carried out in these frequencies as a result of research interest in satellite applications.
The active devices considered in this review are: HEMTs, pHEMTs, mHEMTs, BJTs and HBTs. Since we focus on power applications, the active devices under study mostly falls (with some exceptions) in the group of high voltage devices. The need for high efficiency operation makes the choice of high voltage devices a highly recommendable practice, although the same power could be achieved with lower voltage devices.

Table 3.3 shows typical operating and breakdown voltages for the current state of art devices [24]:

Device	Breakdown Voltage (V)	Operating Voltage (V)	Output Power (W)	Gain (dB)	Efficiency (%)
Si BJT	63	36	110	7.4	40
Si LDMOS	70	28	100	13	55
GaAs MESFET	60	28	300	14	63
SiC MESFET	90	40	56	10	55
GaAs pHEMT	50	26	43	11.5	56
SiC GaN HEMT	80	48	370	10	50
GaAs HBT	70	28	20	11	70

Table 3.3: Comparison of Devices at 2.1GHz(From [24])

Among the advantages for high voltage operation we can mention that operation above 20V decreases the DC-DC conversion power loss and the bias interconnect I^2R power loss. The design of input and output matching networks becomes simpler due to higher power density and higher load impedance, respectively. This also leads to greater bandwidths.

As a rule of thumb GaN HEMT and other transistors such as GaAs FET and GaAs HEMT have similar input impedance per unit gate width. However, the output impedance is about twice for the same unit gate width. Thus, if a device has 10 times higher power density capacity means that will require 10 times smaller input and 20 times smaller output impedance transformation ratio.

Figures 3.2 and 3.3 show how the breakdown voltage is related with the cut off frequency and power density (output power) capabilities, respectively. In due course this issues shall considered more deeply.

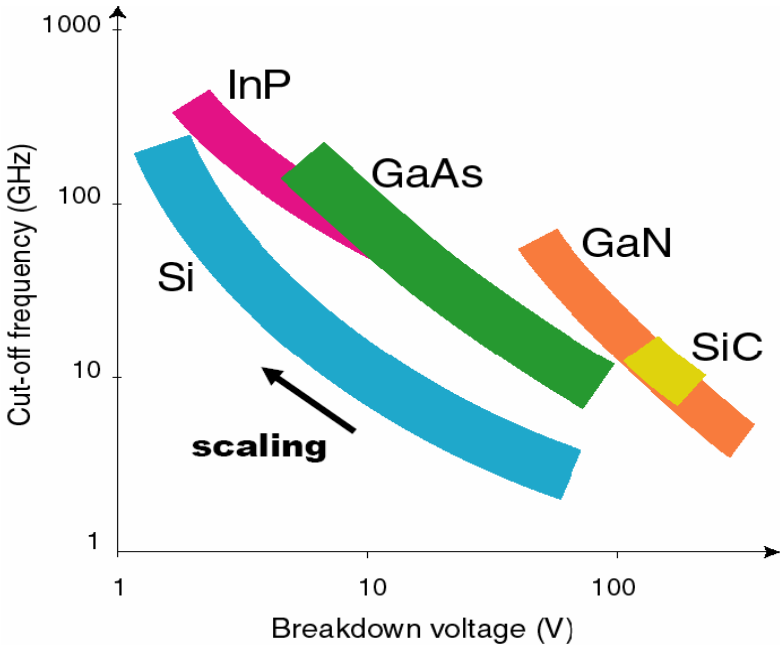


Figure 3.2: Trade off between Voltage and Frequency. (From [3])

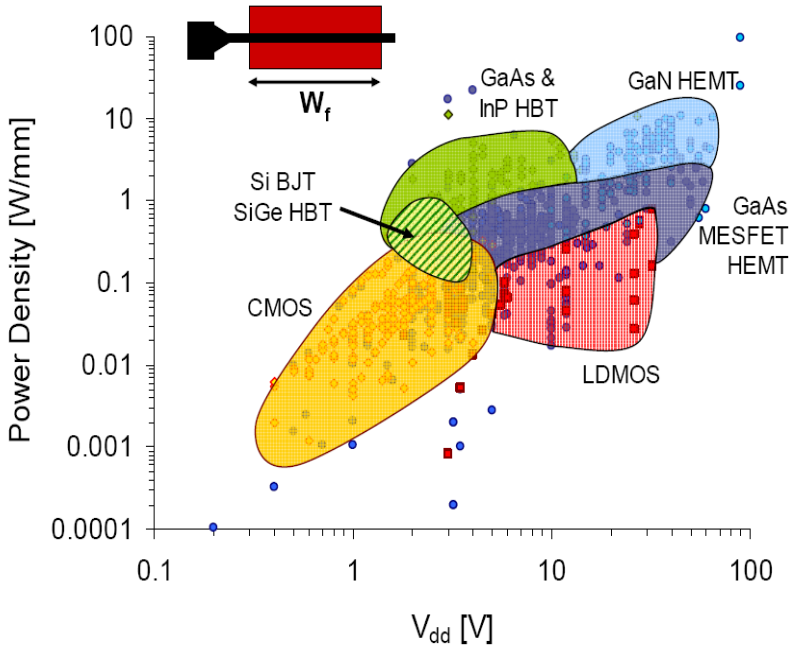


Figure 3.3: Trade off between Voltage and power density. (From [3])

In the next sections, we present a detailed description of the active devices considered.

3.3.1 GaN on SiC HEMTs

BACKGROUND

The concept of HEMT was first introduced in 1978 [65] after successful experiment on modulation-doped AlGaAs/GaAs heterostructure . In HEMT devices, electrons from remote donors in a higher band gap material transfer to adjacent lower gap material. The electrostatics of the heterojunction results in the formation of a triangular quantum well at the interface, which confines the electrons in a two dimensional (2D) electron gas (2DEG). The separation of the 2DEG from the ionized donors significantly reduces ionized impurity scattering resulting in high electron mobility and saturation velocity.

This devices were first called Modulation Doped Field Effect Transistors (MODFET) although the name of HEMT remained. Earlier HEMTs utilized the AlGaAs/GaAs system, which was the most widely studied and best understood heterojunction system at that time. It consisted of a single heterojunction. Since then, other material have been used. For example a double heterojunction HEMTs, such as AlGaAs/InGaAs/GaAs have also been introduced (Figure 3.4). This figure shows a single and double heterojunction devices. In the case of single heterjounction, the substrate is usually the same material as the channel , whereas in double heterojunction the channel layer is sandwiched between an upper and lower barrier layer. The first experimental device was reported by Fujitsu researchers in 1980 [66]. The device was based on AlGaAs/GaAs heterostructure. The HEMT devices also was named as MODFET, TEGFET, HFET and HJFET.

The first commercial application of a HEMT came from an unexpected application. In 1983 Fujitsu demonstrated a four stage HEMT amplifier operating at 20GHz [67] which works as low noise amplifier at Nobeyama Radio Observatory in Nagano (Japan).

The first mass market application of AlGaAs/GaAs HEMTs came in the communication arena after the recognition of their superior high frequency noise characteristics over MESFETs. They enabled a reduction in antenna size by one half. By 1988, the annual world wide fabrication of HEMTs receivers was about 20 million [68].

The High Electron Mobility Transistor (HEMT) can be found in several substrates such as: SiC, Si, sapphire or GaN. Although the most notably today is the SiC substrate.

The progress in such devices was possible due to the advances in crystal growth techniques such as Molecular Beam Epitaxy (MBE) and Metal-Organic Chemical Vapor Deposition (MOCVD). The progress is related also to the advances in device processing techniques, most notably the Electron Beam Lithography, which enabled the fabrication of HEMT with gate lengths down to $0.05\mu m$.

ACTIVE DEVICE DESCRIPTION

The fabrication of GaN HEMT s is similar to that for the GaAs pHEMTs of the following section. A major difference is in the AlGaN/GaN materials, which have high field breakdown, giving rise to high voltage operation of GaN HEMTs. The high electron mobility of GaN layers allows the highest power density among all active devices. SiC based HEMT have the highest power density followed by Si based HEMT. Because SiC is a good electrical insulator, the SiC Gan HEMT process is very suitable for IC production due to low-loss matching circuitry.

Typical values for GaN devices are showed below in table 3.4:

I_{max}	I_{dss}	g_m	f_T	f_{max}
$900mA/mm$	$600mA/mm$	$290mS/mm$	50GHz	80GHz

Table 3.4: GaN Typical Values

Power densities of $10W/mm$ for 4GHz and $5W/mm$ for 35GHz has been demonstrated. Drain voltage operation as high as 65V has been reported.
A theoretical limit for the power density in GaN HEMT is approximately given by [69]:

$$P_O \cong 7\frac{V_{ds}}{28} \tag{3.1}$$

From equation 3.1 it can be observed the importance of the high voltage operation capability.

In HEMT devices different material are grown (one on top of the other) using epitaxial growth technology like molecular beam epitaxy (MBE) or molecular organic chemical vapor deposition (MOVCD). There are different variations of HEMT. One of the most usual structure used versions is shown in Figure 3.4. This device has a layer of aluminum gallium arsenide (AlGaAs), which has large energy bandgap than GaAs, grown on top the GaAs semi insulating substrate layer.
NOTE: Figure 3.4 refers to the earlier HEMTs designs [65]. They were today commercially replaced by slightly different AlGaAs/GaAs structures of layers that derived in the so-called pHEMT device (see next section). In turn that device has a similar operating principle than HEMT. The most advanced AlGaAs/GaAs HEMT can be found in the Japanese industry (i.e. [70]). However the current device mainstream is the AlGaN/GaN HEMT which fully replaced the former one.

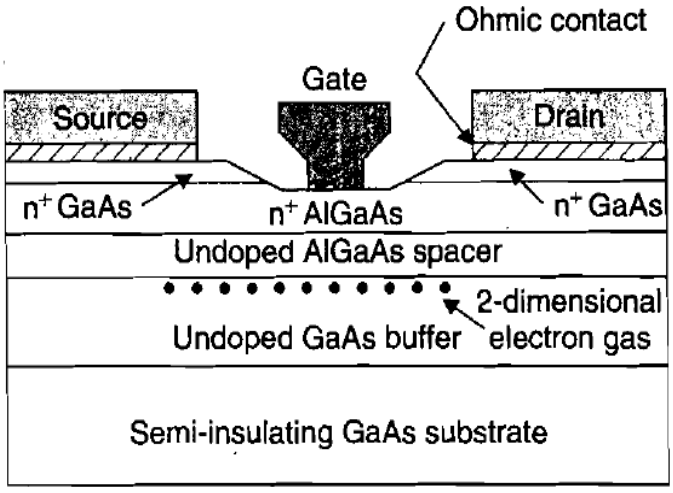


Figure 3.4: AlGaAs/GaAs HEMT Structure

The operating principle of the HEMTs is related to the difference in the Fermi energies between two materials that causes band bending at the heterojunction interface (see Figure 3.5) when they are joined. This band bending results in a quantum well where a large population of electron forms a two dimensional electron gas (2DEG) very close to the interface of the two materials. This electron gas is responsible for high current density and high electron velocities.

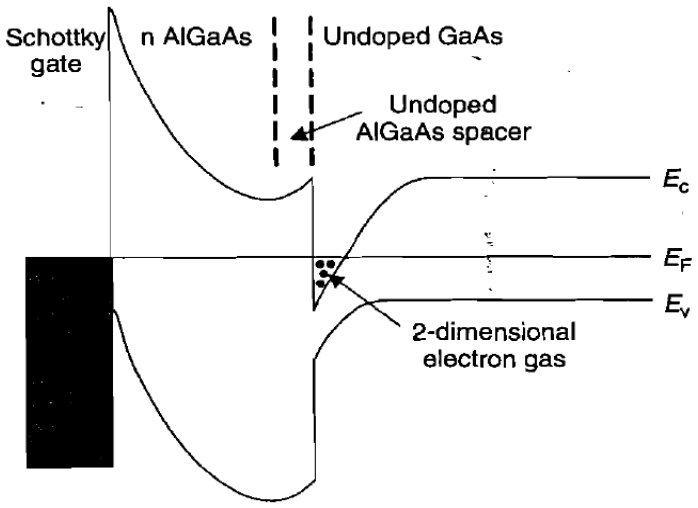


Figure 3.5: AlGaAs/GaAs HEMT Energy bands

In order to increase the charge density of the 2DEG zone, for power transistors, multiple quantum wells are usually realized, as for instance depicted in Figure 3.6 [71]. Moreover, to avoid scattering phenomena occurring between the electrons in the 2DEG and ionized donors, is customary to add an undoped AlGaAs (namely spacer layer) between the n-type AlGaAs and the undoped GaAs [57].

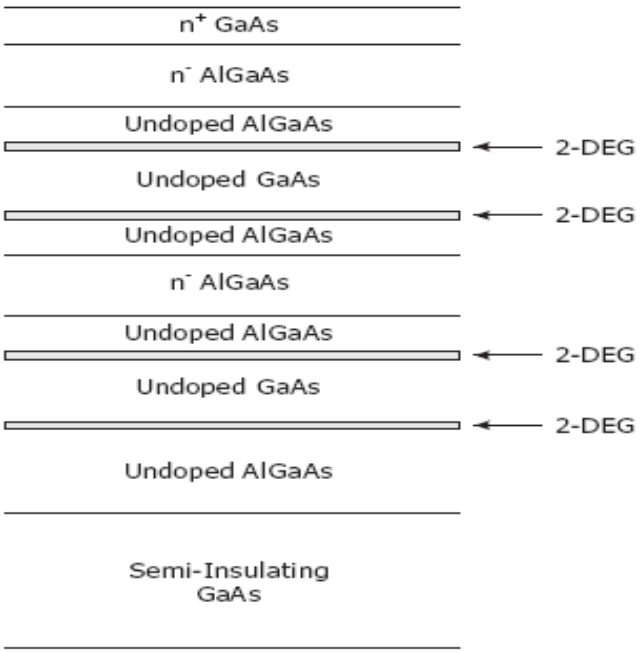


Figure 3.6: Multiple quantum well HEMT structure

As mentioned previously, there are two main types of HEMTs, AlGaAs/GaAs based and AlGaN/GaN based (InP based is still under research phase). Next we present a brief description of their main features.

- *Power AlGaAs/GaAs HEMT Features.*
  The layer structure of this device is depicted in Figure 3.4. Maximum drain current of 200-650mA/mm and gate-drain breakdown voltages of around 10-20V are usual. Recent work, however, has led to significantly improved breakdown voltages. Both gate-drain and source-drain breakdown voltages above 30V have been obtained [70], and very high gate drain breakdown voltage of 47V has been realized [72].
  Typical output power density are in the range of 0.5 to 1.5 W/mm at frequencies up to 40GHz. At 1.5GHz, a maximum of 1.7 W/mm has been reported [72]. This kind of HEMT delivers higher power density compared to GaAs MESFET. AlGaAs/GaAs HEMT can deliver 0.4W/mm output power at 60GHz [73].High power designs are presented in [74], [75].

- *Power AlGan/GaN HEMT Features.*
  The structure of AlGaN/GaN HEMTs is similar to that of the AlGaAs/GaAs HEMTs discussed in previous sections (Figure 3.4). It consist, from top to bottom , of cap, barrier, channel and buffer layer, grown on the substrates mentioned before (Si, SiC or sapphire), see Figure 3.7.

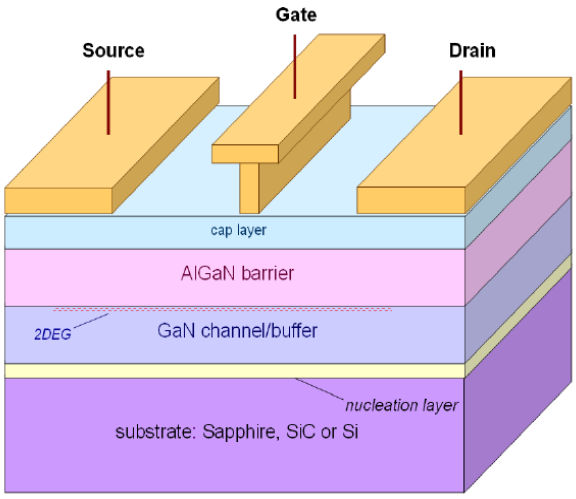


Figure 3.7: AlGaN/ GaN HEMT basic structure.

There are more than one configuration possible for layer structures. Figure 3.8 shows a couple of them.

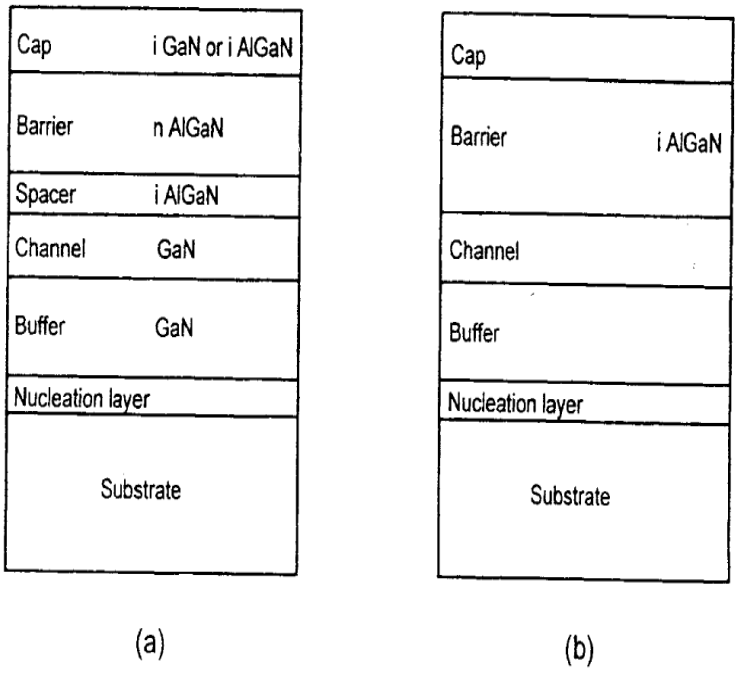


Figure 3.8: AlGaN/ GaN layer sequences. (a) with doped barrier layer, and (b) with undoped barrier layer

The Figure 3.8 (a) employs a doped AlGaN barrier layer above the channel, whereas undoped bar-

rier layer is used in the structure of Figure 3.8 (b). The working differences caused by doped or undoped barrier can be found in [54].

Typically AlGaN/GaN HEMTs show maximum drain currents I_{max} well above 1000mA/mm and extrinsic transconductance g_m between 200 and 300 mS/mm. The best reported values are 1430 mA/mm and 300 mS/mm for I_{max} and g_m respectively [76], [77]. AlGaN/GaN HEMT exhibits extremely high breakdown voltages. Typical values of the gate drain breakdown voltages are between 60V and 200V, a record of 284V has been reported in [39]. Values as high as 107GHz for f_T and 155GHz for f_{max}have been demonstrated [78].

Most AlGaN/GaN HEMT development have been focused on high power transistors. Power densities of 10.7W/mm at 10GHz [79] and 12.1 W/mm at 3.5 GHz [80]. Researchers of Triquint demonstrated a 4W/mm HEMT devices at 35GHz [81]. Cree 's research team showed a 9.4W/mm power density at 10GHz for AlGaN/GaN HEMT on GaN substrate [82] but up to date they do not offer commercially GaN o GaN foundry process.

ACTIVE DEVICE and MMIC RESEARCH

Very promising results up to 35GHz were demonstrated by GaN HEMT technology [69], [83], [84], [85], [86], [87], [88], [89]. They can be attributed to high breakdown field and saturation velocity, which are both higher as compared to GaAs. Resulting power density is about ten times than that demonstrated in GaAs. Thus, for a given output power, the device size is reduced by same factor. Smaller devices tend to decrease the requirement a need for power combiners. Both reduce the chip area and improve matching circuit design. The most promising results for GaN have been achieved on SiC substrates. Those made of sapphire provide less power and power density, due to lower thermal conductivity of this substrate material. An example is the low power design at 21GHz [86].

Because the relative immaturity of GaN with respect to GaAs, reliability and yield issues still remain open.

Next, tables 3.5 and 3.6 shows a list of the most novel MMIC designs up to date.

Output Power $Watts$	Freq. Band	Power Density W/mm^2	Eff. %	Gain in dB	Number of Active Devices	Materials	Foundry	Company or Institution	Year
4	Ka	3.3	23	11	3	AlGaN GaN on SiC	Rockwell	Rockwell Scientific	2006 [90]
5	Ka	3.3	23	12	3	AlGaN GaN on SiC	Rockell	Rockwell Scientific	2006 [87]
5	C	5	35	6	2	AlGaN GaN on SiC	Univ. Chalmers	Politec. Torino	2010 [91]
16	X	1.9	30	18	3	AlGaN GaN on SiC	IAF	FBH	2006 [6]
20	X	1.1	30	16	12	AlGaN GaN on SiC	Selex	Tor Vergata	2008 [92]
50	X	3.25	30	19	12	AlGaN GaN on SiC	Selex	Tor Vergata	2010 [4]
43	X	4	52	10	6	AlGaN GaN on SiC	UMS	Alcatel Thales	2010 [93]
11	X	5	N/A	10	3	AlGaN GaN on SiC	Nanging Inst.	Nanging Inst.	2007 [5]
20	X	1.11	40	15	6	AlGaN GaN on SiC	UMS	Alcatel Thales	2010 [94]
11	K	3.5	52	10	10	AlGaN GaN on SiC	Triquint	Triquint	2010 [95]
58	X	3.22	38	8	6	AlGaN GaN on SiC	UMS	Alcatel Thales	2008 [7]
20	X	2.9	25	18	4	AlGaN GaN on SiC	Fraunhofer Inst.	Fraunhofer Inst.	2006 [96]
20	X	N/A	N/A	14	5	AlGaN GaN on SiC	Selex	Selex	2009 [97]
3.5	Ka	N/A	26	8	N/A	AlGaN GaN on SiC	Cree	Cree	2003 [85]
0.04	K	N/A	N/A	15	2	AlGan GaN on sapphire	Matsushita Elect.	Matsushita Elect.	2005 [86]
...	...	...	...	...	...	...	...	...	...

Table 3.5: State of Art of HEMT MMIC - Research.

...	...	...	...	...	...	...	...	...	...
Output Power $Watts$	Freq. Band	Power Density W/mm^2	Eff. %	Gain in dB	Number of Active Devices	Materials	Foundry	Company or Institution	Year
10	X	0.9	N/A	12	N/A	AlGaN GaN on SiC	Hebei Semicon.	Hebei Semicon.	2008 [98]
20	X	1.66	40	12	6	AlGaN GaN on SiC	Fraunhofer	EADS Daimler	2006 [99]
25	X	1.81	21	15	N/A	AlGaN GaN on Si	Nitronex	Triquint	2005 [100]
9	X	0.66	25	20	N/A	AlGaN GaN on SiC	Fraunhofer	Fraunhofer	2005 [101]
1.7	W	1.2	20	21	14	AlGaN GaN on SiC	Raytheon	Raytheon	2011 [102]
5	Ka	3.1	20	13	6	AlGaN GaN on SiC	Rockwell	Rockwell	2006 [88]
2.8	Ka	2.3	27	8	6	AlGaN GaN on SiC	HRL Labs.	HRL Labs.	2004 [89]

Table 3.6: State of Art of HEMT MMIC - Research. Cont...

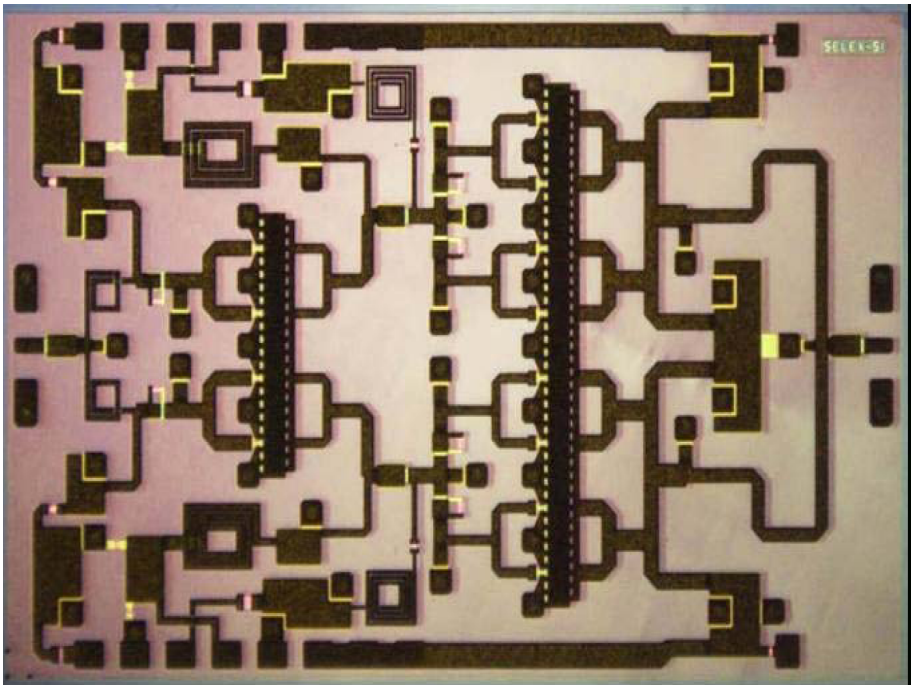


Figure 3.9: 50W, X-Band, GaN HEMT MMIC power amp. (chip size: 5.0mm x 3.2mm ([4])

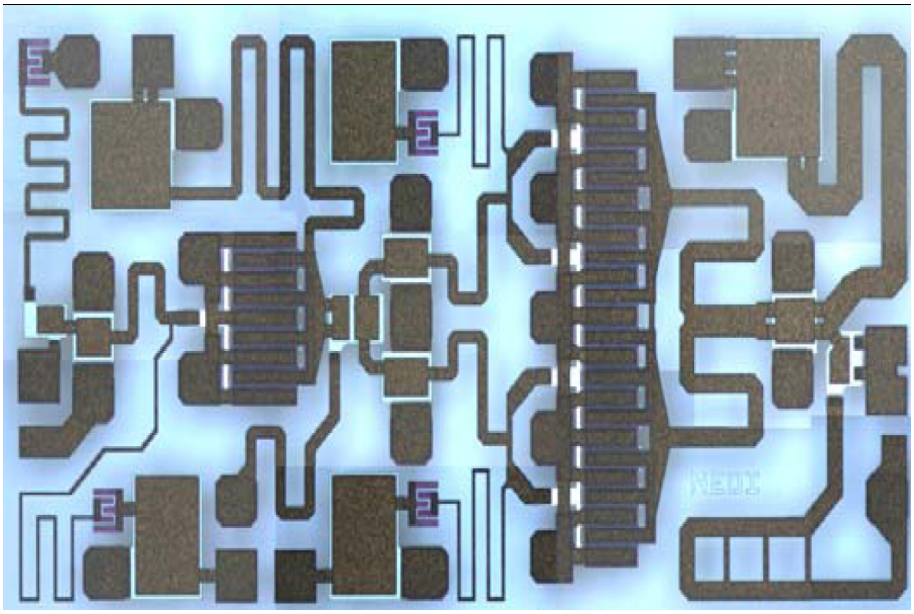


Figure 3.10: 11W, X-Band, GaN HEMT MMIC power amp. (chip size: 2.0mm x 1.1mm ([5])

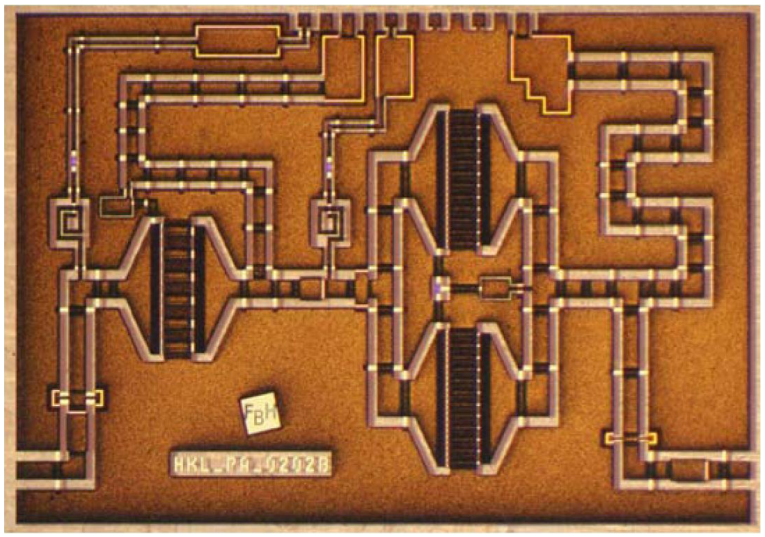


Figure 3.11: 16W, X-Band, GaN HEMT MMIC power amp. (chip size: 2.2mm x 3.3mm ([6])

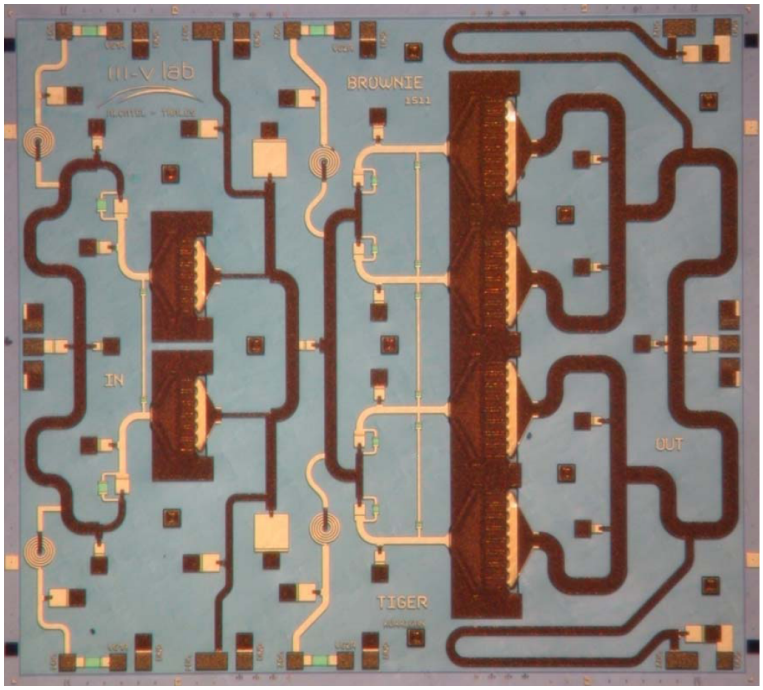


Figure 3.12: 58W, X-Band, GaN HEMT MMIC power amp. (chip size: 4.0mm x 4.5mm ([7])

Next figures(7.3, 7.4, 3.15 and 3.16) shows graphically the information previously presented in tables 3.5 and 3.6:

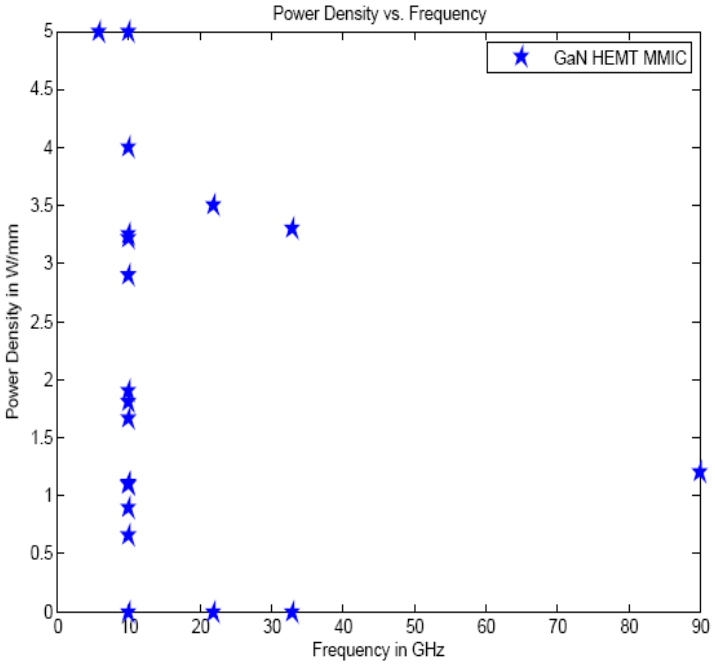


Figure 3.13: GaN HEMT State of Art. Power Density

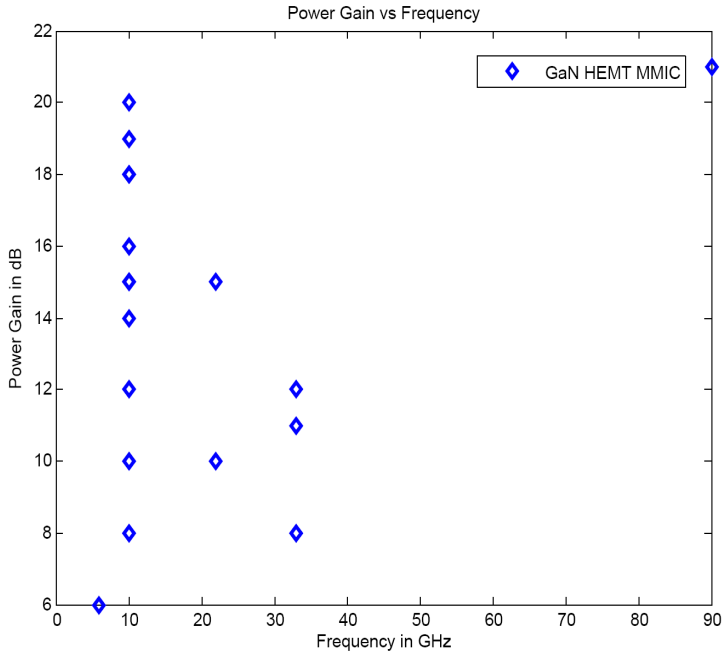


Figure 3.14: GaN HEMT State of Art. Gain

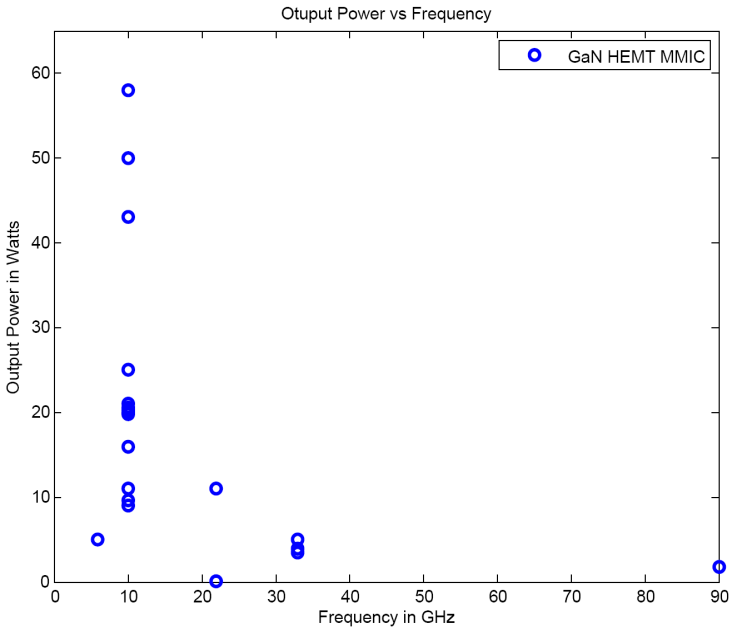


Figure 3.15: GaN HEMT State of Art. Output Power

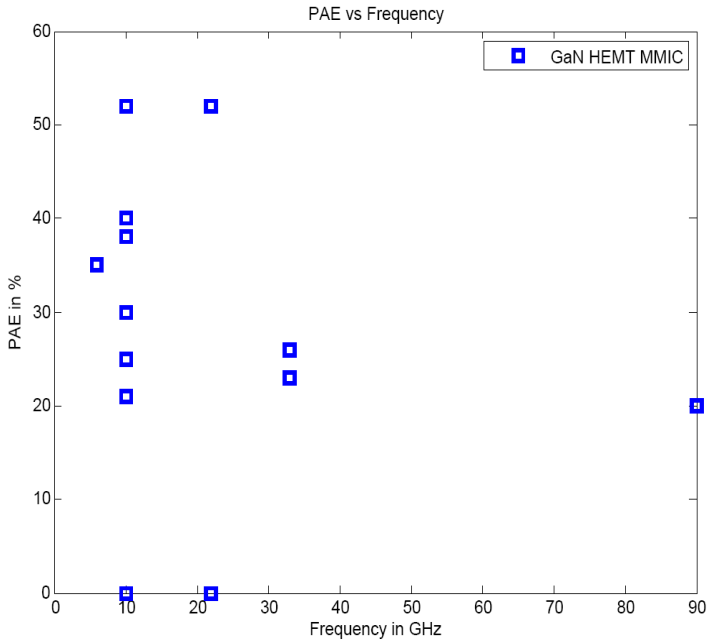


Figure 3.16: GaN HEMT State of Art. PAE

NOTE: In previous Figures those values equal to zero refers to non available data from form published works (See Tables 3.5 and 3.6).

ACTIVE DEVICE and MMIC COMMERCIAL PRODUCTS.

GaN industry is divided in three worldwide regions, EUA, Japan and Europe. Asia (Taiwan or China) still do not have presence different to what happens with Si or GaAs industry.

The most advanced, proven and available products comes from EUA. Japan, in turn, is almost at the same level of technological development than EUA but not many open commercial foundries can be found. Europe is at the beginning of commercialization, at our knowledge only one foundry sells GaN foundry process. The details for this introduction are presented next. The concepts also involve aspects of the academic world as described in previous paragraph.

- GaN in EUA.

  The emerging GaN technology in EUA is pushed by DARPA Agency. The main objective of this initiative is to realize higher efficiency and larger power density monolithic microwave integrated circuits than are possible using GaAs, InP or SiGe transistors. This program works under the umbrella of the *DARPA GaN Technology Thrust* formed by major GaN companies in USA and the academic institutions of the same country.

  The program started in early 2000s and follows the same structure that those carried out for GaAs technology in early 1990s by the same agency.

The program is organized in 3 phases and 3 tracks [103]. Phase I of the program is focused upon achieving low defect, high resistivity SiC substrates and improved GaN based epitaxial layer structures. This program phase is highly successful and culminated in the availability of 3 inches diameter SiC substrates. Phase II, started in early 2005 with a plan to continue through 2008, realizes high yield of reliable, high performance GaN based devices. Following phase III, planned for the two next years, will produce high performance MMICs and will demonstrates their use in several types of modules.
The program has three distinct performance track for the all the mentioned phases. These tracks are established to demonstrate the versatility of the devices and MMICs. The track focus on developing the following modules:

- Track I relates to an X band transmitter /receiver module containing a power amplifier and a low noise amplifier. Raytheon is the leading contractor which feature an alliance with Cree Inc.
- Track II focused on a 40GHz band high power amplifier modules: it is headed up by Northrop Grumman Space Technologies.
- Track III requires the development of high bandwidth (2GHz-20GHz) high power amplifier module. In this phase Triquint works with BAE, Nitronex and Academic partners to take charge of this track at beginning of 2005.

All three tracks used Silicon Carbide as a substrate. At the moment the program has developed GaN HEMTS for high power electronics resulting in sufficiently mature transistors to confidently predict $> 10e6$ hours of MTTF for up to 40GHz power devices operation [104]. The DARPA project actualy also achieve the main objective of bringing to market commercial GaN products and foundry services, giving at EUA a clear leadership in the state of art for GaN technology.
Table 3.7 shows a not exhaustive list of GaN players in EUA at the end of year 2010:

Item	Players
Substrate	AXT Inc., Cree Inc., Kyma Technologies.
Epitaxy	Spectrolab, AET, ATMI, Bandwidth Semiconductor Inc., Cermet, EMCORE.
Devices and Process	Triquint, BAE, Northrop Grumman, RFMD, Raytheon.
Circuit Design	AMCOM, Gain Microwave, Custom MMIC, Skyarna, RFNTech, RFMD, Triquint.
Characterizations	Triquint, BAE, RFMD, Raytheon, Northrop Grumman

Table 3.7: GaN players in EUA

Today, Cree, Nitronex, RFMD and Triquint are the main providers of the foundry process. At least the main of 'commercial' since others like Northrop Grumman or BAE systems (among

others) only work under EUA's government agencies contracts.
Cree and Nitronex are pure GaN players, RFMD and Triquint grows as GaAs foundries adding GaN process a few years ago. Even when they are not pure GaN players they are strongly competing in GaN arena.

- GaN in Japan.
  The model of GaN industry in Japan followed a different path than in EUA. Most of the companies adopted the strategy of work in a closed form (only for japanese market) in all the supply chain. So they do not offer foundry services (or other services) to third parties if they are outside Japan, even when they handle the state of art in the technology. For example, Nippon Sanso, Nissin Electric or Anelva can build any type of epitaxy system required by customer. However, these companies are known for restricting their business within Japan [105].
  Some of milestones in GaN development that were done by Japan companies are: Nichia Chemical Industries reported the first GaN blue laser diode at the beginning of 1996 (blue LEDs were the first applications of GaN substrates). Fujitsu developed in 2005 the first HEMT with isolated gate technology which allowed output power of 100Watt or greater [106]. In 2010 Sumitomo Electric developed the first 6-inch GaN wafer substrate for manufacturing white LEDs [107]. This company was a provider of foundry services and process but no longer offers this option. Instead, they offer designed and manufactured discrete devices. Hitachi and Sony also played a key role in the industry development due their R&D developed in house.
  Were not able to find foundry process and foundry services providers of GaN power transistor or MMICs design in this country.

- GaN in Europe.
  Europe has a long history on the development of III-V technologies. In particular, some of the GaAs pioneering work, like the co-invention of the HEMT device. Over the last years the focus has strongly shifted to GaN based devices and a large community including academia, industry and national research institutes is now strongly involved in the development of GaN devices and technologies. Although in the last decade Japan and EUA have mostly been in the limelight (in particular with the first products being put on market) significant and innovative work has also been done in Europe reaching the state of the art.
  There are two major federating projects that today supports GaN research. One is named the *Korrigan Initiative* (supported by the European Defense Agency (EDA) [108]), it covers all aspects from substrates to modules. The other one is called *GREAT* (supported by the European Space Agency (ESA) [109]). This project focuses on reliability improvement for space applications. The final objective is clearly to achieve a complete, independent and open food chain for the GaN technology.
  In parallel to a fully open commercial offer, some companies, mainly in the defense sector (EADS, Thales, Selex SI, QinetiQ for instance) keep internal resources operation to address specific needs through their own R&D centers(Thales with ATL III-V Lab, Selex, etc...) or through specific

partnership (EADS with IAF, etc...)
The mainstream pointed in Europe is based on AlGaN/GaN HEMT on SiC substrates but other alternatives like InAlN/GaN (for high temperature applications UltraGaN [110] or MorGaN [111]) are under study.
The following table shows a not exhaustive list of GaN players in Europe at the end of year 2010:

Item	Players
Substrate	Soitec, Norstel.
Epitaxy	Picogia, QinetiQ, Azzuro, ATL II-V Lab, IMEC, IAF, FBH, Ulm Univ., Chalmers Univ., FORTH, EPFL, CRHEA, etc.
Devices and Process	UMS, OMMIC, IAF, FBH, ATL II-V Lab., Ulm Univ., Qinetiq, RWTH Aachen, MicroGaN, NXP, IMEC, IEM, IET, Slex, Chalmers, etc.
Circtuit Design	IAF, FBH, EADS, Thales, UMS, TESAT, Alcatel Lucent, Qinetiq, SAAB, Ericsson, Selex, AMS, TNO,ATL III-V Lab, IEMN, etc.
Module and Systems	Thales, EADS, IAF, NXP, TNO, Qinetiq, Salex, Alcatel Lucent, Astrium, etc.
Characterizations	Bristol Univ, CDTR, UMS, IAF, ATL III-V Lab, FBH, IEMN, Padova Univ., Tor Vergata Univ., IRCOM, XLIM, ISOM, DEI, MFA, IMS, etc.

Table 3.8: GaN players in Europe

Related to the current feasibility project, OMMIC is the only foundry in Europe that offers a GaN process under the denomination of D01GH (presented in EuMW 2009). On the other side, NXP launched a GaN discrete product (CLF1G0530-50) based in UMS technology (presented at IMS2011), but at October 2011. Either UMS or NXP, do not offer an open GaN foundry process in their foundry product portfolio.

Table 3.9 shows the GaN foundry process available today.

Process Name	Foundry	Country	f_t GHz	Power Density W/mm	Gate μm
$0.25\mu m$ GaN 3MI	Triquint	EUA	32	7	0.25
NRF1	Nitronex	EUA	6	N/A	0.5
GaN HEMT MMIC	Cree Inc.	EUA	8	4	0.4
GaN1	RFMD	EUA	11	8	0.5
GaN2	RFMD	EUA	9	4	0.5
D01GH	OMMIC	Europe	90	N/A	0.1

Table 3.9: State of Art of commercially available GaN HEMT foundry process

Once described the GaN industry state or art, we present the following table 3.10 where the most representative GaN commercial products are detailed.

Name	Output Power ($Watts$)	Freq. Band (GHz)	PAE	Gain in dB	Type of Device	Company
CMPA801B025D	25	8-11		28	MMIC	Cree Inc.
CMPA5585025F	25	5.5-8.5	30	20	MMIC	Cree Inc.
CGH60060D	60	DC-6	65	15	Bare Die	Cree Inc.
CGH60120D	120	DC-6	65	12	Bare Die	Cree Inc.
T1G6001528-Q3	18	DC-6	60	10	Transistor	Triquint
TGF2023-01	6	DC-12	55	15	Die	Triquint
TGF2023-05	25	DC-12	55	17.8	Die	Triquint
TGF2023-10	50	DC-18	47	8.9	Transistor	Triquint
TGF2023-20	90	DC-12	55	17.5	Die	Triquint
TGA2573	10	2-18	25	9	MMIC	Triquint
RF3932D	60	DC-4	68	14	Die	RFMD
RF3933	90	DC-3	65	13.5	Tr	RFMD
RF3930D	10	DC-4	70	19	Die	RFMD
RF3934D	120	DC-4	60	12	Die	RFMD
MAGX-000035-150000	60	DC-3.5	N/A	25	Transistor	MACOM
CHK015A	15	DC-6	45	14	Transistor	UMS

Table 3.10: State of Art of HEMT Devices and MMIC - Commercial Products

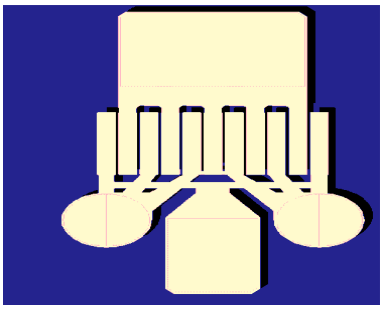


Figure 3.17: TGf2023-01 Layout (6W)

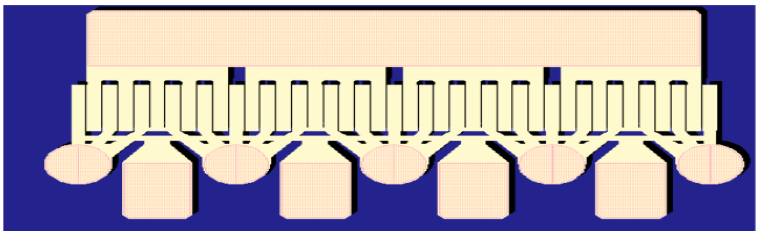


Figure 3.18: TGF2023-05 Layout (25W)

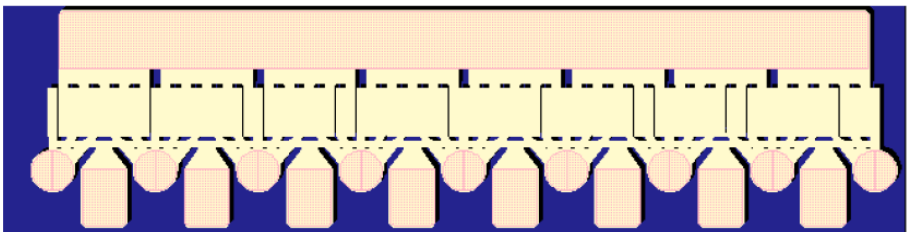


Figure 3.19: TGF2023-10 Layout (50W)

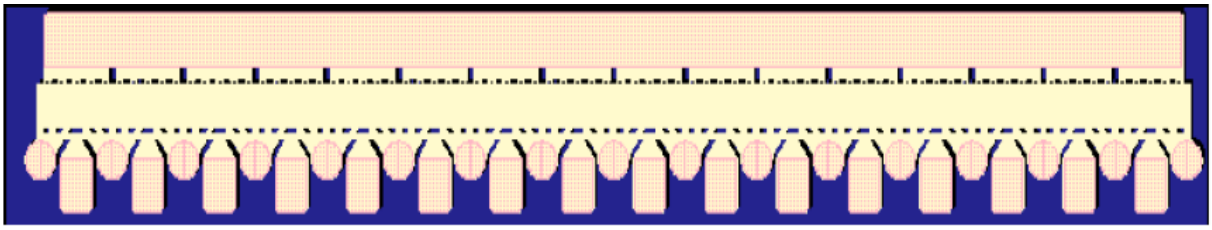


Figure 3.20: TGF2023-20 Layout (90W)

SUMMARY.
From the previous paragraph we can obtain certain preliminary conclusions:

- The mainstream for GaN HEMT is the AlGaN/GaN on Sic combination for layers and substrate respectively.
- Four commercial foundries are available in USA and one in Europe. Japan, although being in the state of art, do no offer foundry services.
- All the GaN HEMT technologies up to date exceed by far the X band frequency requirements of the current feasibility study.
- Several research prototypes circuits on GaN MMICs that surpasses the frequency and power requirements have been found.
- GaN Discrete and GaN MMICs commercial products that achieve the frequency and power requirements have been found. However, above 8GHz, the number of products is reduced substantially, which highlight the complexity of designs at these frequencies.
- To achieve the power requirements of this feasibility study multi transistor circuits designs shall be considered.
- Reliability aspects still remain as an issue to be improved.

3.3.2 GaAs pHEMTs

BACKGROUND
The 80s produced two key innovations that would help greatly to expand the high frequency capabilities of GaAs based HEMTs. The first one was done by Ketterson et al. in 1985 [112]. In this work was demonstrated by the first time the *Pseudomorphic HEMT* device concept using an AlGaAs/InGaAs/GaAs quantum well structure (InGaAs is the channel structure). The second innovation was done by Chao [113]. In his work demonstrated a planar doping of the AlGaAs. This allowed the thinning down of barrier yielding improvements in transconductance, channel aspect ratio and device scalability.
PHEMT device works in a similar fashion that HEMT of previous section, the only difference is the heterostructure layer. PHEMT is today the device of choice in GaAs and InP substrates, leaving HEMT only constrained to SiC substrates.

The extraordinary capabilities of pHEMT in terms of noise, power, and low-loss switching at very high frequencies made this device technology a success in the commercial arena (TV,DBS,GPS,RADAR,Fiber Optics,etc).
PHEMT IC technology is today manufactured around the world on 6-inch GaAs wafers and is available in foundry mode from several companies. This technology is following in last decade a similar path to Si

technologies (like BiCMOS). Thus, are emerging techniques to monolithically integrated enhancement and depletion mode devices, HBTs, and high quality passive elements to enable enhanced functionality single chips systems [114]. This makes possible the development of highly integrated front-end modules for high volume cellular phone applications.
In the past few years, GaAs pHEMT has emerged as a device of choice for implementing microwave and millimeter wave power amplifiers. Breakdown voltage, the key parameter for power devices, typically ranges from 8V to 15V in current state of art devices.
Reliability requirements for space applications are typically (measured as a mean-time-to-failure (MMTF)) in the order of $10^7 h$ (or 1142 years) at channel temperature of $125 C\circ$.

ACTIVE DEVICE DESCRIPTION

The basic layer structure of GaAs pHEMT consists (Figure 3.21) from the top of: a cap layer, a barrier layer, a spacer , a channel, buffer, and a substrate.

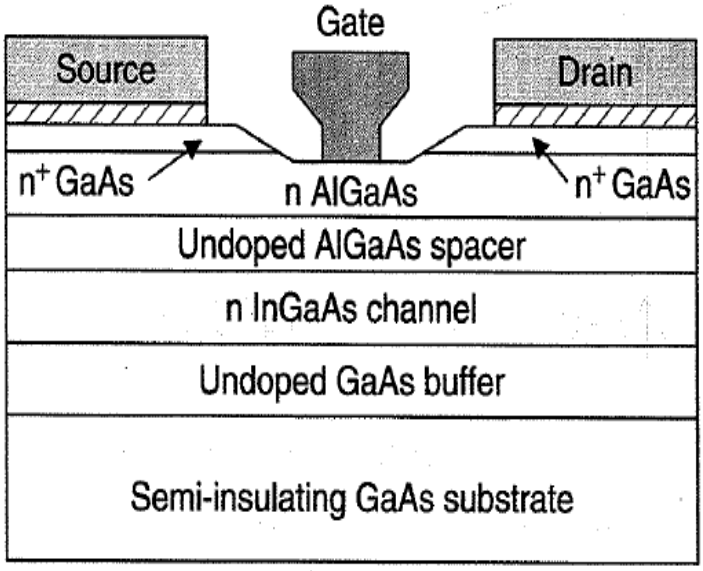


Figure 3.21: GaAs pHEMT layers structure

The thin channel layer is composed of a pseudomorphic InGaAs alloy, which is sandwiched between the spacer and the underlying buffer. The principle of functioning is the same described for HEMT in previous section. There are variations from the basic structure (Figure 3.22) with different layers configurations.

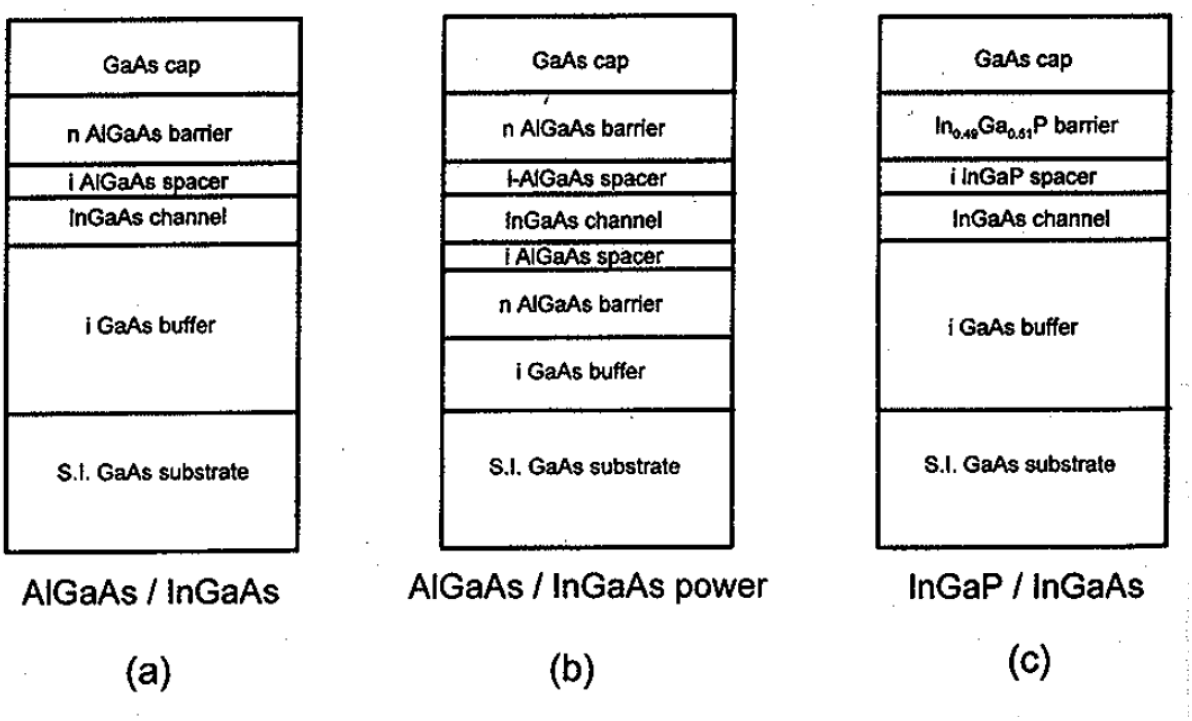


Figure 3.22: Layer Sequences:(a)Conventional GaAs pHEMT, (b) GaAs pHEMT with two electron supply layers, and (c) GaAs pHEMT with InGaP barrier layer

Looking at Figure 3.22 the configuration (b) shows favorable characteristics for power transistors construction since has two electrons supply layers above and below the InGaAs channel. This increases the channel sheet density and decrease the On channel resistance. Configurations (a) and (b) are the most accepted today by foundry companies. For example, these layer structures are used by: UMS, Triquint, RFMD, OMMIC and GCS. Configuration (c) is only used by Win Semiconductor.

Power GaAs pHEMTs are widely used in the frequency range from 1GHz to tents of GHz. A meaningful power amplification at frequencies high as 94GHz has been achieved. The maximum drain current is typically 500-800 mA, which is considerably higher than that of AlGaAs/GaAs HEMTs. Record of I_{max} of 1000mA/mm has been demonstrated [115].
One of the most important innovation in power pHEMT devices was the invention of the Field Plate which is a modification of the structure that allows the increasing of output power through an increasing in the breakdown voltage.
Typical values for pHEMT devices are showed below in table 3.11:

I_{max}	I_{dss}	g_m	f_T	f_{max}
$335mA/mm$	$204mA/mm$	$180mS/mm$	6GHz	28GHz

Table 3.11: GaAs pHEMT Typical Values

For a 32mm device, output power of 43W and PAE of 56% can be obtained. At X band frequencies output power of 20W-25W have been demonstrated (see next section).

ACTIVE DEVICE and MMIC RESEARCH.

There is no doubt that the most widespread technology makes use of GaAs based pseudomorphic HEMTs. They dominates the mm-wave bands up to 50GHz, while recent advances in GaN HEMTs dominate at lower frequencies. The commercial amplifier, TGA4915 from Triquint, delivers a record output power of 7Wat 27GHz. The highest power pHEMT MMICs operating around 45GHz [116] and 60GHz [117] have been reported.

During a first half of 90's pHMET has overtaken the role from MESFET as the most powerful technology at this time. The only MESFET power MMIC found to be published after year 2000 is the 13GH solution from M/A-COM [118].

Next, tables 3.12 and 3.13 shows a list of the most novel MMIC designs up to date.

Output Power $Watts$	Freq. Band	Power Density W/mm^2	Eff. %	Gain in dB	Number of Active Devices	Materials	Foundry	Company or Institution	Year
1	Ka	.4	17	15	8	AlGaAs/InGaAs on GaAs	UMS	Nanowave Inc.	2003 [119]
3.8	Ka	.7	36	9	28	AlGaAs/InGaAs on GaAs	Triquint	Triquint	2010 [120]
10	X	.72	33	40	14	AlGaAs/InGaAs on GaAs	N/A	Taiwan Univ.	2007 [8]
10	X	.58	40	13	12	AlGaAs/InGaAs on GaAs	Win Semi-cond.	TNO Defence	[121]
.663	Ka	0.07	57	15	20	AlGaAs/InGaAs on GaAs	Triquint	Triquint	2009 [122]
8	X	N/A	N/A	35	4	AlGaAs/InGaAs on GaAs	UMS	SpA Microwave	2011 [123]
0.3	C	0.2	22	25.6	6	AlGaAs/InGaAs on GaAs	OMMIC	Univ. Hong Kong	[124]
0.5	X	.7	65	6	1	AlGaAs/InGaAs on GaAs	RFMD	Selex, QinetiQ	2011 [125]
17	C	0.48	45	25	12	AlGaAs/InGaAs on GaAs	UMS	UMS	2009 [126]
8	X	0.48	30	17	12	AlGaAs/InGaAs on GaAs	Selex	Selex	2007 [127]
1	X	0.13	44	5	2	AlGaAs/InGaAs on GaAs	Selex	Tor Vergata Univ.	2010 [128]
10	Ku	0.53	47	12	12	AlGaAs/InGaAs on GaAs	Triquint	MEC , Thales Alenia, Bologna Univ.,	2008 [11]
...	...	...	...	...	...	...	...	...	...

Table 3.12: State of Art of pHEMT MMIC - Research.

... Output Power $Watts$	... Freq. Band	... Power Density W/mm^2	... Eff. %	... Gain in dB	... Number of Active Devices	... Materials	... Foundry	... Company or Institution	... Year
8	S	2.1	64	14	2	AlGaAs/InGaAs on GaAs	Triquint	Triquint	2007 [100]
1.6	Ku	N/A	42	11.5	4	AlGaAs/InGaAs on GaAs	UMS	XLIM, ESA	2011 [129]
6.5	Ka	0.22	25	23	30	AlGaAs/InGaAs on GaAs	Win Semicond.	Mimix	2008 [130]
8	C	2.5	35	19.5	10	AlGaAs/InGaAs on GaAs	Selex	Alcatel Alenia	2006 [127]
1	Ka	1.2	52	8.5	1	AlGaAs/InGaAs on GaAs	Triquint	Triquint	2010 [131]
1	K	0.16	27	10	6	AlGaAs/InGaAs on GaAs	Win Semicond.	Tor Vergata	2008 [132]
5	X	0.38	25	19.5	13	AlGaAs/InGaAs on GaAs	Win Semicond.	TNO Defence	2007 [9]
12	X	0.88	42	17.5	10	AlGaAs/InGaAs on GaAs	N/A	Taiwan Univ.	2008 [8]
3.5	X	0.22	49	10	6	AlGaAs/InGaAs on GaAs	Raytheon	Raytheon	1996 [133]
8	X	0.55	45	18	10	AlGaAs/InGaAs on GaAs	UMS	UMS	2008 [10]
3.2	X	0.15	50	24	7	AlGaAs/InGaAs on GaAs	Raytheon	Raytheon	2000 [134]
10	X	0.47	40	16	12	AlGaAs/InGaAs on GaAs	Filtronic	Filtronic	2005 [135]
9	X	0.56	35	20	12	AlGaAs/InGaAs on GaAs	Fraunhofer Inst.	TNO Physics Lab.	1999 [136]
5	X	0.63	55	11	10	AlGaAs/InGaAs on GaAs	N/A	Hughes Aircraft	1996 [137]
...	...	...	...	...	...	...	...	...	...

Table 3.13: State of Art of pHEMT MMIC - Research. Cont.

... Output Power $Watts$	... Freq. Band	... Power Density W/mm^2	... Eff. %	... Gain in dB	... Number of Active Devices	... Materials	... Foundry	... Company or Institution	... Year
3.2	Ka	0.91	14	26	8	AlGaAs/InGaAs on GaAs	Win Semicond.	Mimix	2007 [138].
3	Q	0.20	25	22	38	AlGaAs/InGaAs on GaAs	Raytheon	Raytheon	2006 [117]
9	Ku	0.81	30	12	12	AlGaAs/InGaAs on GaAs	N/A	Transcom Inc.	2006 [139]
6.5	Ku	0.76	24.6	10.5	12	AlGaAs/InGaAs on GaAs	N/A	Transcom Inc.	2007 [140]
3	Ka	0.23	N/A	21.5	26	AlGaAs/InGaAs on GaAs	Triquint	Triquint TGA4501	2002 [141]
0.8	Ku	0.43	23.5	21	4	AlGaAs/InGaAs on GaAs	OMMIC	Zhengzhou Univ.	2007 [142]
0.2	Ku	0.06	31	32	3	AlGaAs/InGaAs on GaAs	Win Semiconductor	TM Innovation Centre	2010 [143]
2	Ka/Q	0.26	N/A	21	20	AlGaAs/InGaAs on GaAs	Triquint	Triquint TGA4515	2004 [5]
6	Q	0.2	17	9	12	AlGaAs/InGaAs on GaAs	Mitsubishi	Mitsubishi	2010 [144]

Table 3.14: State of Art of pHEMT MMIC - Research. Cont.

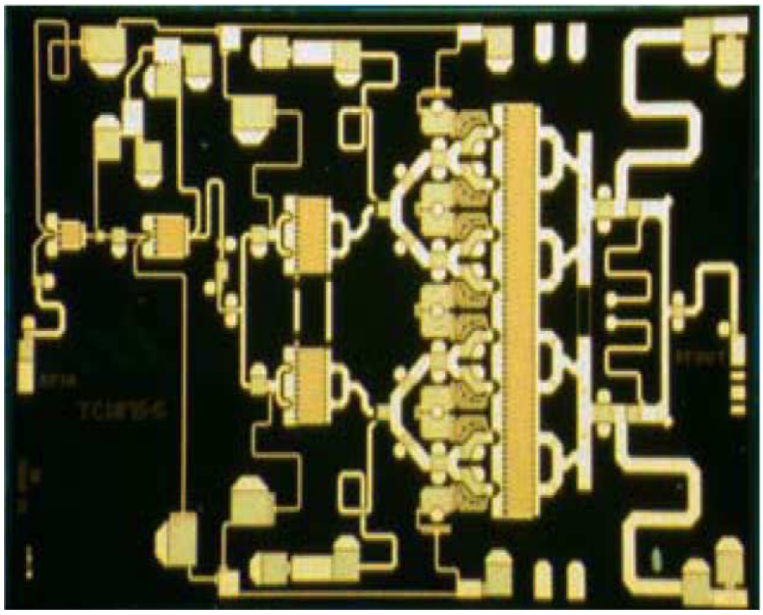


Figure 3.23: 10W, X Band, InGaAs pHEMT MMIC power amp. (chip size: 4mm x 3.45mm [8])

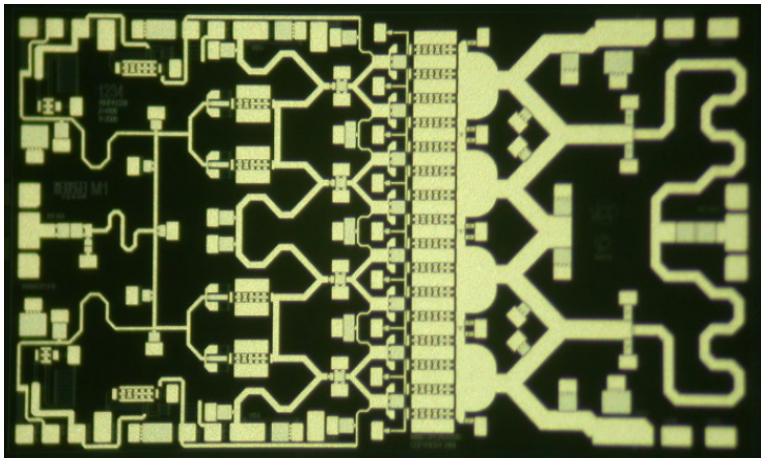


Figure 3.24: 10W, X Band, InGaAs pHEMT MMIC power amp. (chip size: 4.41mm x 2.5mm [9])

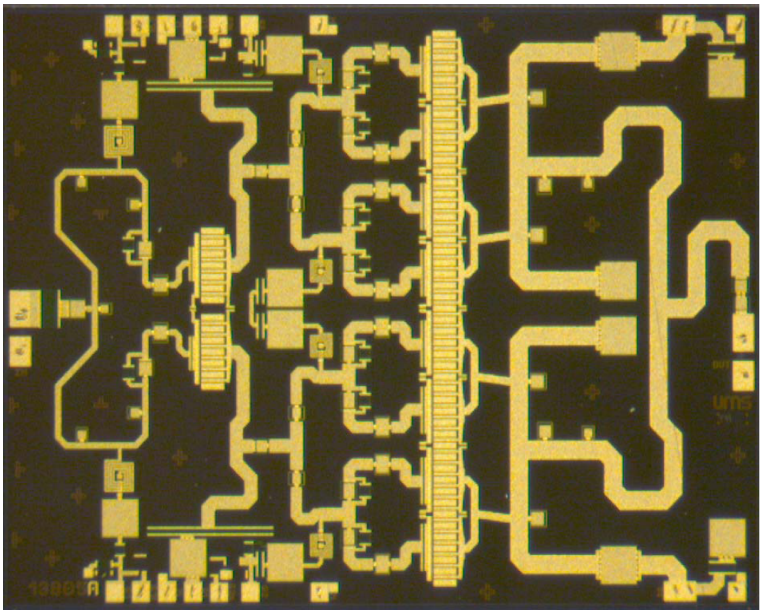


Figure 3.25: 8W, X Band, InGaAs pHEMT MMIC power amp. (chip size: 4.41mm x 3.31mm [10])

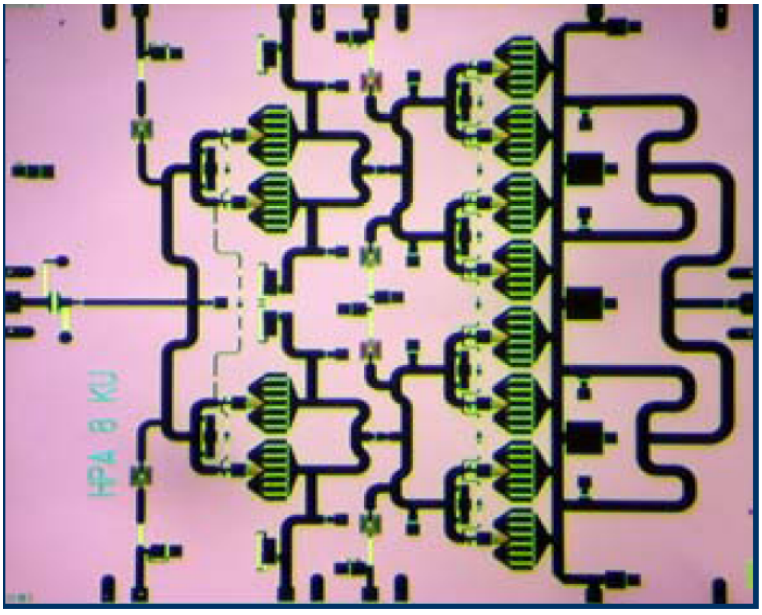


Figure 3.26: 10W, X Band, InGaAs pHEMT MMIC power amp. (chip size: 4.7mm x 4mm [11])

Next figures(7.1, 7.2, 3.29 and 3.30) shows graphically the information previously presented in tables 3.12, 3.13 and 3.14:

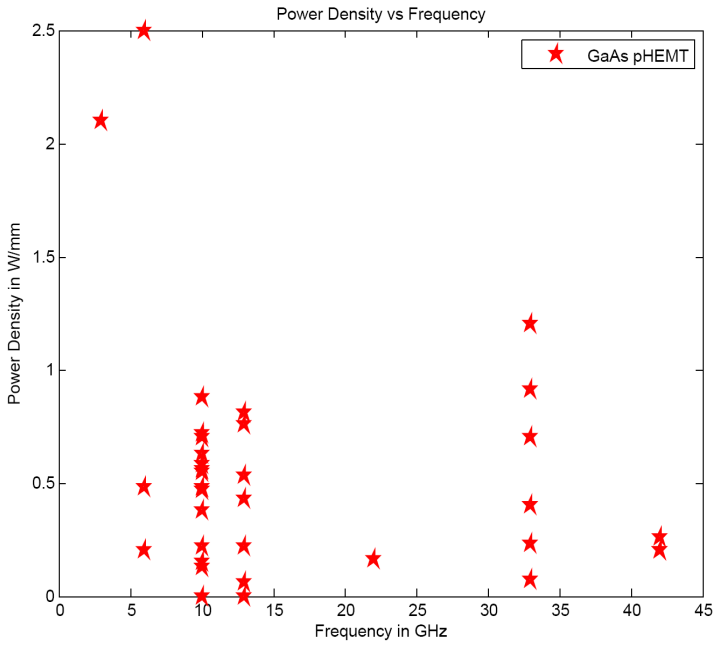


Figure 3.27: GaAs pHEMT State of Art. Power Density

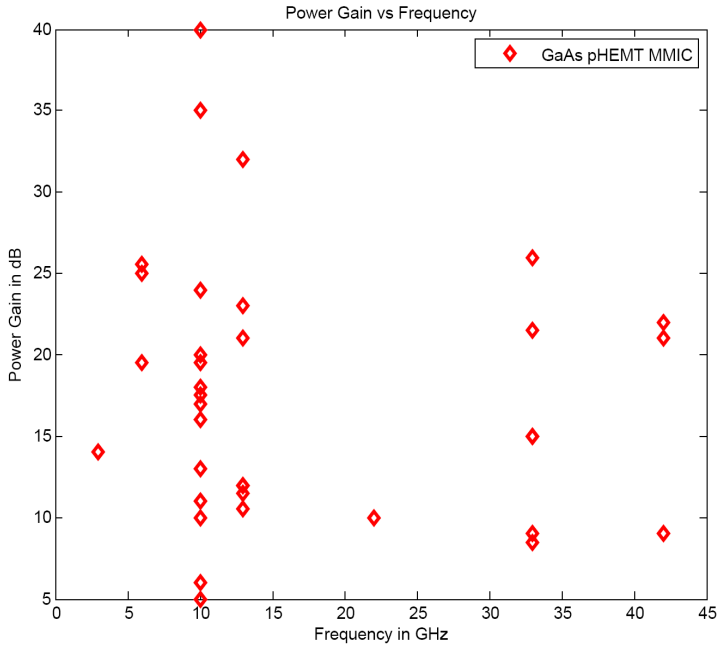


Figure 3.28: GaAs pHEMT State of Art. Gain

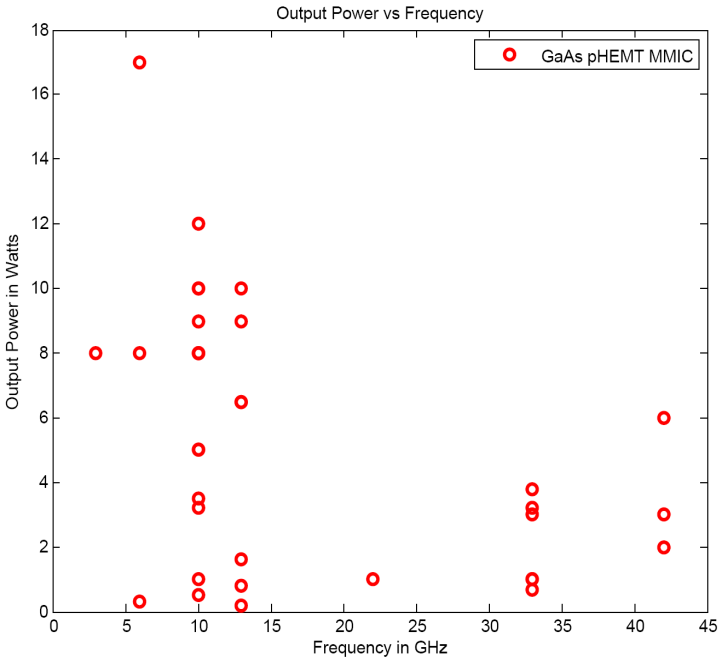


Figure 3.29: GaAs pHEMT State of Art. Output Power

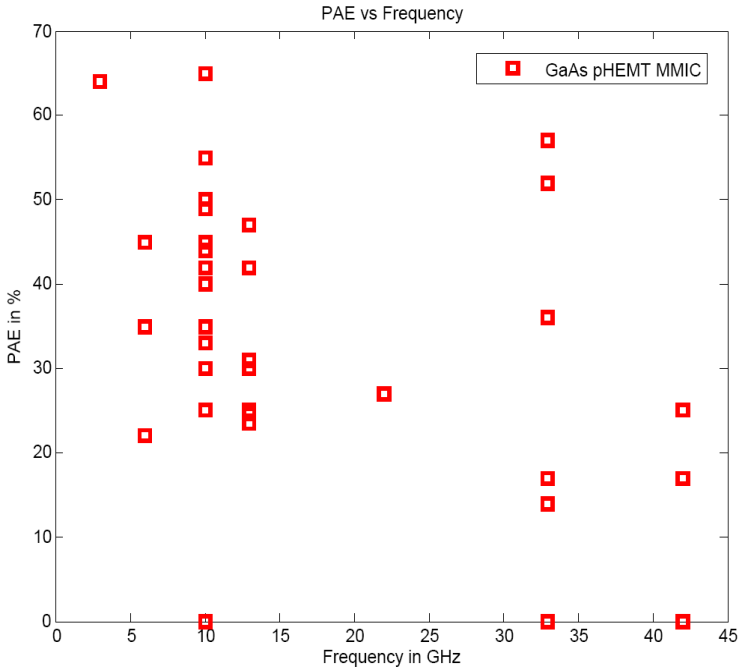


Figure 3.30: GaAs pHEMT State of Art. PAE

NOTE: In previous Figures those values equal to zero refers to non available data from published works (See Table 3.12 and 3.13).

ACTIVE DEVICE and COMMERCIAL PRODUCTS.

In the 1980s, the running joke was 'GaAs is the future and always will be'. Until that time it was a great promise, but its potential performance was plagued by high material costs an inconsistent process. However, due to a large investments by the government/military in the 1980s (DARPA MMICs program), and high commercial demand for wireless applications in the 1990s, it has become the mainstay of the RF and microwave industry.

Today most of the high performance commercial wireless products are based on GaAs technology, although GaAs industry is being squeezed by Si and GaN technologies.

The main GaAs foundries in EUA are (not including defense) RFMD and Triquint. In Europe the major foundry services are UMS and OMMIC. Win Semiconductor being a Taiwanese manufactures has its commercial basement in Europe. GCS is also a Taiwanese company. Below we show a list (Table 3.16) of commercial products that can fit in the feasibility study requirements. Most of this products are manufactured by the foundries mentioned previously.

Table 3.15 shows the GaAs pHEMT foundry process available today.

Process Name	Foundry	Country	f_t (GHz)	Power Density (W/mm)	Gate (μm)
$0.35\mu m$ PWR pHEMT 3MI	Triquint	EUA	20	N/A	0.35
$0.25\mu m$ mmW pHEMT 3MI	Triquint	EUA	55	N/A	0.25
$0.15\mu m$ XKu pHEMT 3MI	Triquint	EUA	60	N/A	0.15
$0.15\mu m$ PWR pHEMT 3MI	Triquint	EUA	100	0.78	0.15
TQPED	Triquint	EUA	27	N/A	0.50
TQP25	Triquint	EUA	55	N/A	0.25
TQP15	Triquint	EUA	80	N/A	0.15
TQP13	Triquint	EUA	95	N/A	0.13
FD25	RFMD	UK	50	N/A	0.25
FD30	RFMD	UK	30	N/A	0.30
PPH25	UMS	Germany/France	50	0.70	0.25
PPH25X	UMS	Germany/France	45	0.90	0.25
PPH15	UMS	Germany/France	75	0.60	0.15
PPH15X	UMS	Germany/France	65	0.75	0.15
PH25	UMS	Germany/France	90	0.25	0.25
PH15	UMS	Germany/France	110	0.30	0.25
D01PH	OMMIC	France	78	N/A	0.13
ED02AH	OMMIC	France	60	N/A	0.18
PL15-10	Win Semi.	Europe	95	N/A	0.15
PP15	Win Semi.	Europe	85		0.15
PP50	Win Semi.	Europe	32		0.50
PD50	Win Semi.	Europe	35		0.50
0.25 um PHEMT	GCS	Taiwan	40	N/A	0.25

Table 3.15: State of Art of commercially available GaAs pHEMT foundry process

Name	Output Power ($Watts$)	Freq. Band (GHz)	PAE	Gain in dB	Type of Device	Company
TGF2021-12	16	DC-12	58	11	Bare Die Tr.	Triquint
TGF2022-12	1.25	DC-20	58	13	Bare Die Tr.	Triquint
TGF2022-24	2.5	DC-20	58	13	Bare Die Tr.	Triquint
TGF2022-48	5	DC-20	58	13	Bare Die Tr.	Triquint
TGF2022-60	6.3	DC-20	57	12	Bare Die Tr.	Triquint
TGA2535	2.5	10-12	N/A	25	MMIC	Triquint
TGA4501	2.5	24-31	N/A	23	MMIC	Triquint
TGA2704	6.3	9-10.5	40	20	MMIC	Triquint
CHA7215	9	8.5-11.5	35	28	MMIC	UMS
XP1059	4	13-15	N/A	28	MMIC	Mimix
CHA7114	8	8.5-11.5	40	20	MMIC	UMS

Table 3.16: State of Art of pHEMT Devices and MMICs - Commercial Products

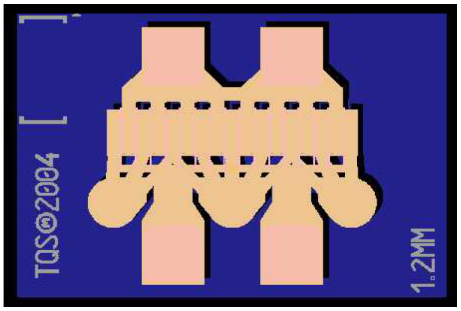


Figure 3.31: TGA2022-12 Layout (1.25W)

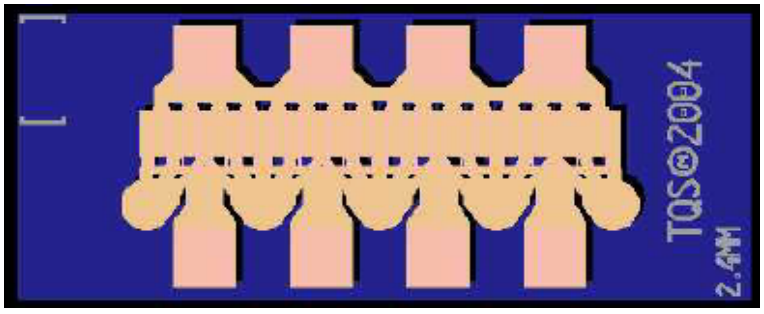


Figure 3.32: TGA2022-24 Layout (2.5W)

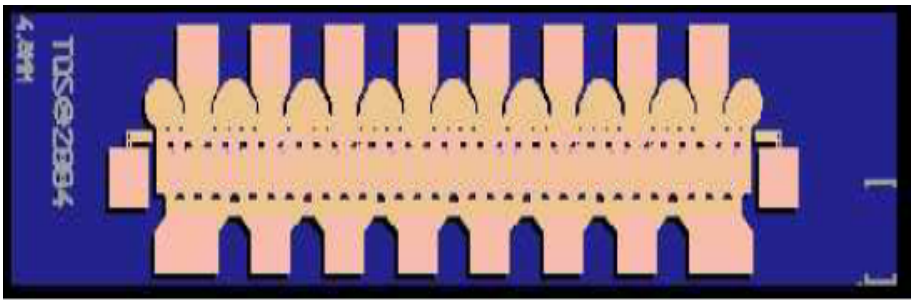


Figure 3.33: TGA2022-48 Layout (5W)

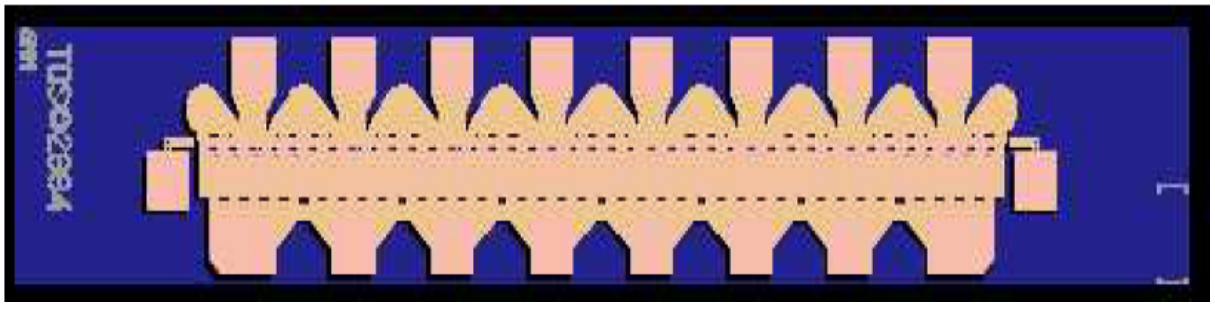


Figure 3.34: TGA2022-60 Layout (6.3W)

SUMMARY.

From the previous paragraph we can obtain certain preliminary conclusions:

- The mainstream for GaAs pHEMT is the AlGaAs/InGaAs on GaAs combination for layers and substrate respectively.
- Two commercial foundries are available in EUA and three in Europe. Taiwan has only one GaAs based foundry.
- All the GaAs based pHEMT technologies up to date exceed by far the X band frequency requirements of the current feasibility study.
- Several research prototype circuits on GaAs MMICs that surpasses the frequency and power requirements have been found.
- GaAs Discrete and GaAs MMICs commercial products that achieve the frequency and power requirements have been found. Different to GaN, above 8GHz, the number of products is acceptable.
- To achieve the power requirements of this feasibility study, multi transistor circuit designs shall be considered. More devices will be needed compared to GaN due to lower power density.
- Reliability aspects are well understood, GaAs technology ages from the beginning of 1990 in the commercial world.

MILESTONES in GaAs pHEMT development from [145]:

- 1951. Heterojunction device proposed by Shockley (U. S. Patent 2.569.347).
- 1969. Mobility enhancement in superlattice heterojunction predicted for GaAs/AlGaAs system [146].
- 1969. Molecular Beam Epitaxy demonstrate [147].
- 1978. Mobility enhancement in GaAs/AlGaAs demonstrated [65].
- 1978. U. S. patent 4.163.237 (for HEMT device) [65].
- 1980. First demonstration of HEMT device. Published latter in [47].
- 1985. Pseudomorphic HEMT introduced [66], [148].
- 1986. Present InGaAs/AlGaAs pHEMT structure introduced. [112] .
- 1987. Pulse doped pHEMT demonstrated [149].
- 1989. First HEMT based MMIC reported at TRW Company.

3.3.3 InP based HEMT and pHEMT

Other variant of HEMT and pHEMT is the manufactured on InP substrates. These devices are commonly build with the following layers: cap (InGaAs), barrier (InAlAs), spacer (InAlAs), channel (InGaAs), buffer (InAlAs) on InP substrate (Figure 3.35). The only difference between HEMT and pHEMT is the content of In in the channel layer.

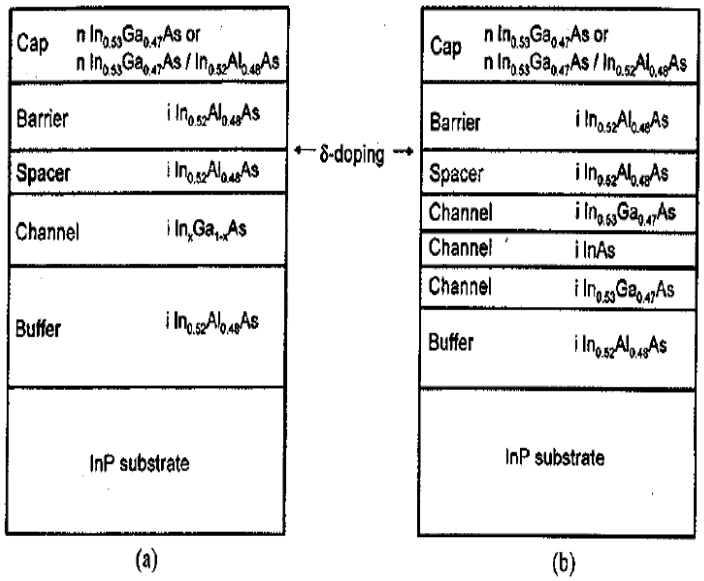


Figure 3.35: InP HEMT layer structure. (a) HEMT, (b) pHEMT

This type of devices have been widely investigated. The technology is developed more slowly than GaAs technology due to the difficulty to growth the material. In general they outperform any other HEMTS in terms of noise figure and cut off frequency. Medium power amplifiers above 100GHz have been presented in [150], [151] and [152]. The technology is less mature than GaAs pHEMT and due to the low breakdown voltage, high power devices are not available.Furthermore, there are not foundry process available for InP based HEMT or InP based pHEMT for power applications. InP based devices are used above 30GHz for low noise application where they do not have competition with other devices.

SUMMARY.

- InP based pHEMT and HEMT are out of scope of present feasibility study. They are devices featured for medium power o low noise amplifier in extremely high frequencies (above 100GHz).
- Not commercial foundries were found for these devices.

3.3.3.1 mHEMT

BACKGROUND

GaAs Metamorphic emerged as an alternative to InP HEMTs [153] and is currently investigated in low nosie amplifiers and medium power amplifiers.

ACTIVE DEVICE DESCRIPTION

The device works in as similar manner as pHEMT or HEMT devices. The only difference is the layers contents and distribution. The layer sequence of GaAs mHEMT is very similar to that of GaAs pHEMTs, but different buffer layer designs have been suggested and employed, Figure 3.36 shows a typical layer for a mHEMT GaAs based device.

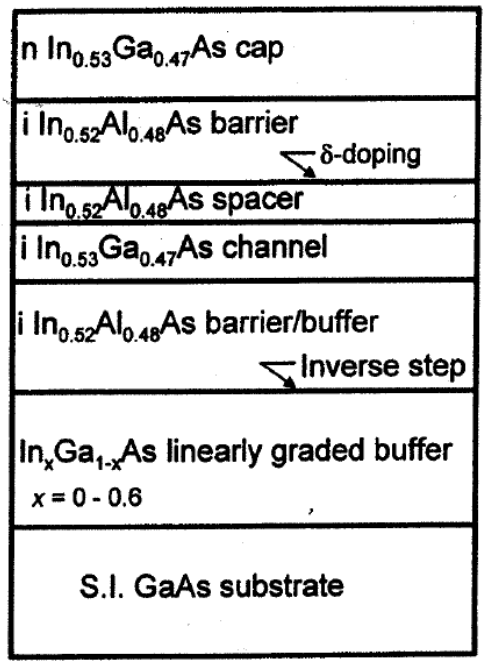


Figure 3.36: GaAs based mHEMT layer typical structure.

DEVICE RESEARCH STATE OF ART

It is well known that InP mHEMTs outperforms GaAs pHEMTs in terms of frequency limits and noise figure. The reason for the superior performance is the enhanced properties of the InGaAs channel with an In content. MHEMTS emerges as an alternative to the costly InP HEMT technology [153] and is currently investigated in low noise applications. Reported output power ([154], [115], [155], [153])are comparable to that achievable in the mature pHEMT technology at Ka-band. Having the advantage of a high gain even at large gate widths [115], the mHEMTS overcome the pHEMTs at W-band. However there is still a lack of research actitives on mHEMT power amplifiers at other frequency bands.

Typical values for GaAs mHEMT devices are shown below in table 3.17:

I_{max}	I_{dss}	g_m	f_T	f_{max}
$900mA/mm$	$600mA/mm$	$1700mS/mm$	204GHz	400GHz [156], [157]

Table 3.17: GaAs mHEMT Typical Values

At present researchers from Raytheon (D. Dumka, W. Hoke, P. Lemonais) together with Triquint team (D. Dumka) and Illinos University (R. Schwindt, G. Cuenva and I. Aseida) claims that mHEMTs will replace all InP based HEMTs and pHEMTs since: cheaper,is available in larger sizes, is less fragile, mature technology for GaAs and commercial potential. They also observed the following critical issues to be solved: robust buffer layer, morphology and reliability issues.
Today a couple of foundries worldwide offers mHEMT process. Triquint has one 0.15-im LN mHEMT 3MI (which is offered as a military product) and OMMIC which have two mHEMT process, D007IH and D01MH. However they are still not released (preliminary release phase). Raytheon and Northrop Grumman have mHEMT process but they are defense companies.

ACTIVE DEVICE and COMMERCIAL PRODUCTS.
Although no power devices are designed with this technology in following table 3.20 we present a brief list of commercial mHEMT products up to day.

Name	Output Power ($Watts$)	Freq. Band (GHz)	PAE	Gain in dB	Type of Device	Company
CGY2190UH	N/A	75-110	N/A	23	Tr	OMMIC
CGY2122XUH	N/A	25-43	N/A	23	Tr	OMMIC
CGY2191UH	N/A	110-160	N/A	20	Tr	OMMIC
TGA4811	N/A	DC-60	N/A	15	MMIC	Triquint
TGA4812	N/A	40GH	N/A	N/A	MMIC	Triquint

Table 3.18: State of Art of mHEMT Devices and MMICs - Commercial Products

SUMMARY.

- The mHEMT devices arise to compete with InP HEMT and InP pHEMT devices. They are out of scope of feasibility study in course. By far surpasses the frequency requirement but they do not offer a this moment enough power capabilities.
- There are foundry process for this technology. Triquint is the only commercial one that provides at this moment. OMMIC is in the preliminary release.

- There are current research activities in MMIC design with this technology. Most of the work are focused above 90GHz frequencies.

3.3.4 Bipolar Junction Transistors

3.3.4.1 Si BJT

Si BJT devices falls out of scope of this feasibility study since their cutoff frequency is below the requirements. In any case, we present a brief overview in order to get more complete perspective of the technologies under discussion .

BACKGROUND

The Bipolar Junction Transistor was the first three terminal semiconductor device capable of delivering signal amplification. After world war II, researchers at Bell Labs were trying to make field effect devices. Although this attempt was unsuccessful, it later led to the birth of the BJT in 1947 [158].

Since early days of BJTs development, device engineers have expended a lot of effort to improve transistor speed and operating frequency. The first transistor capable of amplifying signal at frequencies around 1GHz were Ge BJTs developed in late 1950. Soon after that, the investigation of Si and GaAs based BJTs started. The work on GaAs BJTs had only a limited success, and by 1968 the interest in this transistors had faded and research activities stopped [159]. Research and development of Si BJTs for microwave applications, on the other hand, led to much more fruitful results. By 1963 Si BJTs became competitive with Ge BJT, and by several years was the dominant device for microwave applications [160].

In 1970, the state of art of maximum frequency of oscillation (f_{max}) was around 15GHz. Power BJTs delivered output powers of 100W,20W and 5W at 1GHz, 2GHz and 5GHz respectively [160].

More recently, other microwave transistors such as MESFET, HEMTs and HBTs came in to use, but the BJT microwave device for the range up to 4GHz remained as an important device.

Excellent review of BJTs evolution can be found in [161], [162] and [163].

Today at low and medium powers Si BJTs were entirely replaced by SiGe HBTs considering the complete spectrum [42]. At high power, as mentioned previously, Si BJT is useful.

In year 2000, microwave fabricated in research lab possessed a record f_T of 100GHz [164].

High voltage power version of a microwave BJT consists of a base-emitter multi finger inter digital configuration. The multi cell is comprised of a narrow and long emitter electrodes with emitter ballasting resistors to minimize thermal runaway. The breakdown voltage of such transistors is about 50V-70V. One alternative to the multi finger structure is to use a mesh structure as presented in [165]. The mesh structure consist of a large number of emitter spots. From the device physics point of view, emitter spots acts like an emitter finger, but with reduced self heating effect due to the small dimension.

The reliability of linear class C power BJTs has been well established, with demonstrated MTTF greater than 10^7 hours at 200 Celsius degrees. High voltage device to date can reach a power of 150W (pulsed) at 3GHz.

Table 3.19 shows the most representative state of art commercial products in Si BJT technology.

Name	Output Power ($Watts$)	Freq. Band (GHz)	PAE	Gain in dB	Type of Device	Company
1214-30	30	1.4	20	7	Rs	GHz Technologies
MRF586	1	L	N/A	12	Tr	Adv. Power Technologies
PH1214-30EL	30	L	50	7.8	Tr	M/A COM
PH2731-75L	75	S	38	7.5	Tr	M/A COM
ALR100	100	L	50	6	Tr	Adv. Semicond. Inc.
ASI2226-4	4	S	40	8	Tr.	Adv. Semicond. Inc.
ASI3005	5	S	30	4.5	Tr.	Adv. Semicond. Inc.

Table 3.19: State of Art of Si BJT Devices and MMICs - Commercial Products

SUMMARY.

- Below 4GHz power Si BJT is still an important device.
- Foundry service for Si BJT are available.

3.3.5 Heterojunction Bipolar Transistors

BACKGROUND

The HBT is a bipolar transistor with a basic structure similar to that of Si BJT, discussed in previous section. It has three terminals, namely emitter, base, and collector, and consists of either an *npn* or *pnp* layer sequence. The main difference between the two devices is that in a HBT, the emitter and base are made off different materials, with the bandgap in the emitter being larger than in the base. Thus, the emitter-base junction of an HBT is a heterojunction.

The basic idea to exploit the properties of a heterojunction in bipolar semiconductor devices was first proposed in 1948 by Shockley [158]. In 1957 [48] published a pioneering paper describing the basic theory of the current gain of HBTs. It took, however, many years to put the ideas of Shockley and Kroemer successfully into operational devices. The main drawback was the manufacturing of the device with high quality junctions.

The first reported device was an AlGaAs/GaAs HBT grown by liquid epitaxy in 1970 [160]. The

major breakthrough came from the introduction of two more advanced epitaxial growth methods: molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD). Thanks to these techniques, since 1980s, AlGaAs/GaAs HBT operating at microwave frequencies have been widely investigated and their performance continuously improved. Besides GaAs HBTs, InP HBTs and SiGe HBTs were also investigated during the 1980s and 1990s. InP HBTs are attractive because transistors offer higher frequency limits than GaAs HBTs. SiGe HBTs, on the other hand, paved the way for multi-GHz applications based on the well established and cost effective Si technology.
Experimental results on GaN HBTs, reported by 2001, however, are available only to the dc performance, and no verification of the microwave properties of GaN HBTs was available.
GaAs HBTs with AlGaAs or InGap base have clearly emerged as viable devices for microwave power amplifiers since 1990s.
As mentioned previously, the basic structure of HBTs is similar to that of BJTs. While the BJT consist of only one semiconductor material (Si), the HBT is formed of layers of different semiconductor material. HBTs can be either single heterojucntion (SHBT) or double heterojunction (DHBT). Next table shows the different layers sequences commonly used in and DHBTs.

HBT Type	Emitter	Base	Collector	Subcollector	Substrate	Device
AlGaAs/GaAs	AlGaAs	GaAs	GaAs	GaAs	GaAs	SHBT
InGap/GaAs	InGaP	GaAs	GaAs	GaAs	GaAs	SHBT
InAlAs/InGaAs	InAlAs	InGaAs	InGaAs	InGaAs	InP	SHBT
InAlAs/InGaAs	InAlAs	InGaAs	InP	InGaAs	InP	DHBT
InP/InGaAs	InP	InGaAs	InGaAs	InGaAs	InP	SHBT
InP/InGaAs	InP	InGaAs	InP	InGaAs	InP	DHBT
SiGe	Si	SiGe	Si	Si	Si	DHBT

Table 3.20: Layer sequences of some typical SHBTs and DHBTs

From the feasibility study's perspective all the above HBT devices (AlGaAs, InGaP, Sige and InP) highly exceed the frequency requirements. On the other hand, its power capacity, which depends on the breakdown voltage, varies from one technology to other falling in some cases below fo the power requirements. Figure 3.37, that shows the breakdown voltage relationship with the cutoff frequency for bipolar transistors technology, can help to understand what are the trade offs involved for each HBT technology.

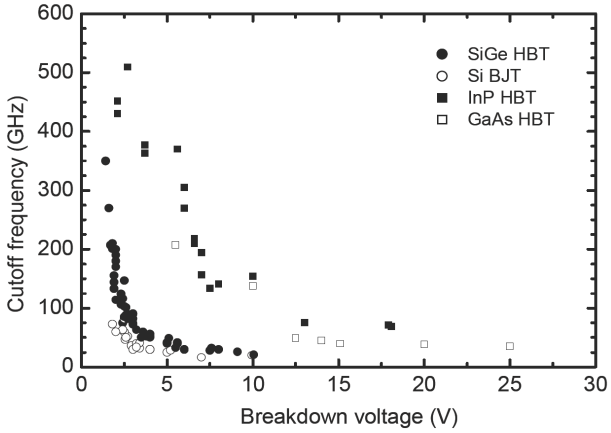


Figure 3.37: Collector-Emitter breakdown Voltage vs Cutoff Frequency (From [12])

3.3.5.1 GaAs HBT

ACTIVE DEVICE DESCRIPTION

As mentioned before today there four two types of GaAs based HBTs: AlGaAs emitter and InGaP emitter Next we present a brief description of the main features for for both devices.

The cross of layer structure of a typical HBT is showed by the next figure 3.38:

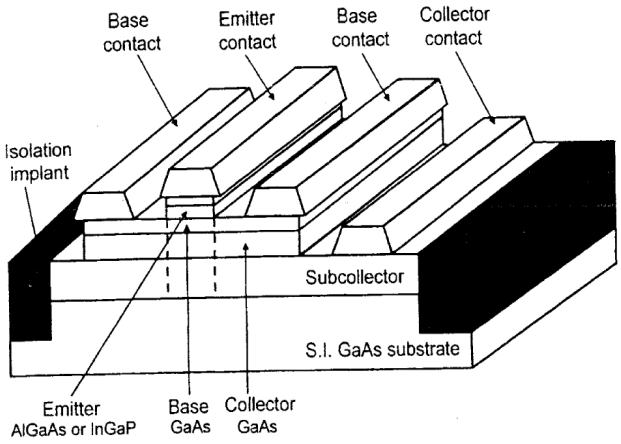


Figure 3.38: Cross section of a typical GaAs HBT

Typical values for AlGaAs/GaAs HBT devices are showed below in table 3.21:

f_T	f_{max}
142GHz	262GHz [166]

Table 3.21: AlGaAs HBT Typical Values

Typical values for InGaP/GaAs HBT devices are showed below in table 3.22:

f_T	f_{max}
156GHz	255GHz [167]

Table 3.22: InGaP HBT Typical Values

Power versions of GaAs HBTs can be operated at 24-28V for high power amplifiers [137], [168] and [169]. Commonly these devices use a relative thicker collector layer in comparison to their low voltage versions. Either AlGaAs or InGaP devices biased a such voltages have demonstrated output power over 20W. The applications of high voltage GaAs HBT are restricted to C band. The high power densities in HBTs give place to considerable self heating, and proper thermal design is critical for such devices.

Below we present a brief description of GaAs based HBTs available today:

- *AlGaAs/GaAs HBT Features.*
  The early experimental an commercial GaAs HBTs [170], [166] employed AlGaAs emitters. This devices are still being widely used for power amplifiers operating at microwave frequencies. The cross section of a typical device was presented in Figure 3.38. It consists it consist of an AlGaAs emitter followed by GaAs base, a GaAs collector and a GaAs sub collector, all mounted on a GaAs substrate.

- *InGaP/GaAs HBT Features.*
  The first InGaP/GaAs HBT was reported in 1985 [171], and in the early 1990s the suitability of these transistors for microwave operation has been established. Since then, InGaP/GaAs HBT has gained increasing popularity. It reached commercial status in the second half of the 1990s and has competing successfully with the AlGaAs/GaAs HBT ever since. The transistor structure is very similar to its AlGaAs counterpart. The only difference is that the emitter change to InGaP materials instead of AlGaAs.
  InGaP/GaAs HBT have several advantages over AlGaAs/GaAs HBT. First the etching solutions for InGaP are selective and do not attack GaAs. Second, InGaP layers contain fewer traps than AlGaAs. Third, the conduction band offset at the ordered InGaP/GaAs heterointerface is almost zero, and most off the bandgap difference appears at the valence band offset. Thus, the ordered InGaP/AlGaAs heterostructure is naturally smooth and no graded layers are required.
  Other crucial advantage is that the life time in InGaP/GaAs is above 20 years, meanwhile for AlGaAs/GaAs this value is around 2 years.

ACTIVE DEVICE and MMIC RESEARCH

We could verify that foundry process are focused on InGaP emitter HBTs (only one foundry in China actually offer AlGaAs). As an example of this situation, references shows research works developed on AlGaAs emitter based devices in early 1990s. See [172], [173] and [174].

For InGaP emitter based devices there are several worldwide companies. In EUA the only commercial foundry is Triquint. RFMD manufactures a plenty number of InGaP devices but they do not offer this process in its foundry service. In Europe: Win Semiconductor and UMS are the only two that provides foundry process for InGaP. In Taiwan we found the following companies: Advance Wireless Semiconductor Company, Compound Semiconductor Manufacturing Co. and Global Communications Semiconductor . The latter is the best positioned among the Taiwanese companies and offers the best services. In China Century Epitech Co. offers wafers for AlGaAs and InGap HBT devices (also HEMT and pHEMT) but they do not provide foundry service to manufacture MMIC.

Next we present the most representative works to unveil the research state of art on InGaP HBT power devices and MMICs.

Output Power $Watts$	Freq. Band	Power Density W/mm^2	Eff. %	Gain in dB	Number of Active Devices	Materials	Foundry	Company or Institution	Year
11	X	0.61	43	16	12	InGap GaAs	UMS	Alcatel Thales	2007 [13]
11	X	0.84	42	15	6	InGap GaAs	UMS	Alcatel Thales	2006 [15]
40	L	3.26	19.5	14.5	10	InGap GaAs	N/A	WJ Communications	2008 [175]
1	L	N/A	N/A	32	N/A	InGap GaAs	N/A	Korea Univ.	2010 [176]
1.8	C	1.3	43	7.6	2	InGap GaAs	N/A	China Univ.	2008 [177]
30	S	9.4	45	12	N/A	InGap GaAs	UMS	Thales	2004 [168]
9	X	0.28	42	13	N/A	InGap GaAs	Daimler Benz Aerospace	Daimler Benz Aerospace	1996 [178]
10	L		65	13	4	InGap GaAs	UMS	Alcatel, CNES	2003 [179]
10	X	N/A	40	14	12	InGap GaAs	UMS	MEC srl, Bologna Univ.	2007 [14]
9.9	X	0.5	33	11	14	InGap GaAs GaAs	Texas	Texas	1994 [180]
10	C	3	50	21	4	InGap GaAs GaAs	UMS	Ericsson	2000 [181]
0.25	C	N/A	30	23	3	InGap GaAs GaAs	Mitsubishi	Mitsubishi	2004 [182]
10	X	N/A	35	16	12	InGap GaAs GaAs	UMS	UMS	2003 [183]
10	X	0.39	30	14	12	InGap GaAs	UMS	Thomson CSF	2000 [184]
9	X	0.31	43	22	8	InGap GaAs GaAs	Daimler Benz Aerospace	Daimler Benz Aerospace	1995 [185]

Table 3.23: State of Art of InGaP HBT MMIC - Research.

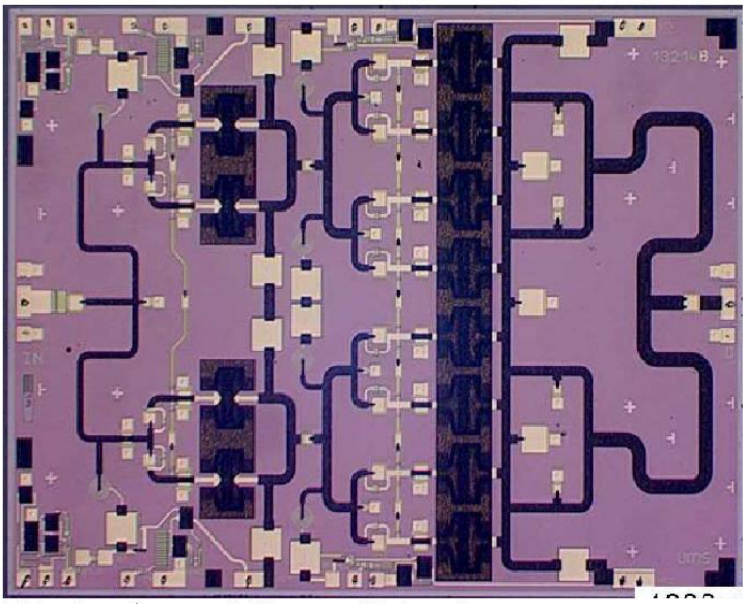


Figure 3.39: 11W, X Band, InGaP HBT MMIC power amp. (chip size: 5mm x 3.68mm [13])

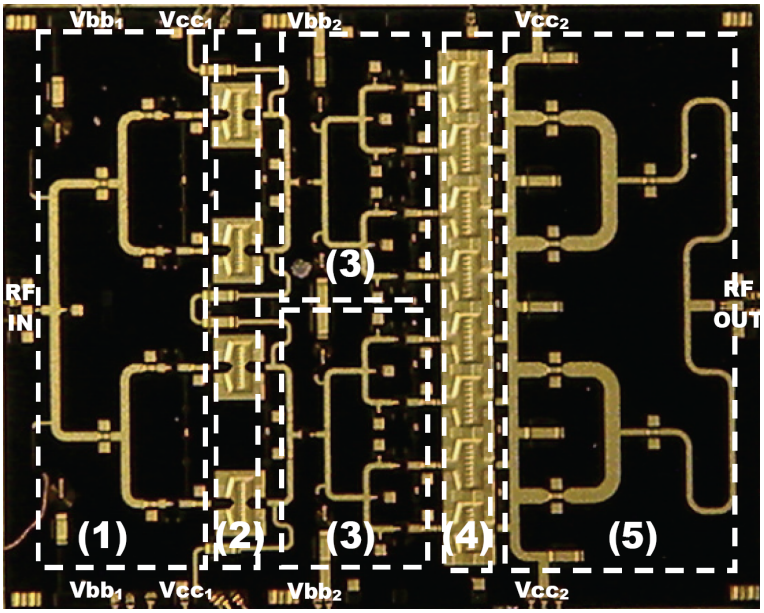


Figure 3.40: 10W, X Band, InGaP HBT MMIC power amp. (chip size: 5.7mm x 4.5mm [14])

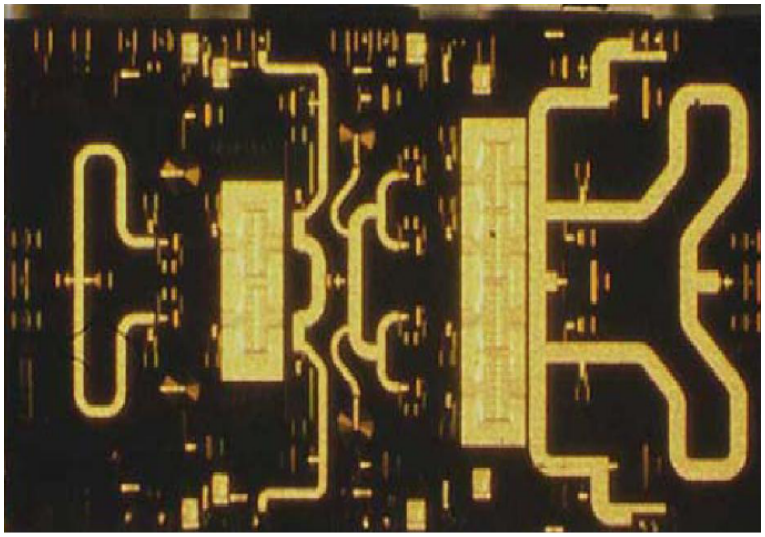


Figure 3.41: 11W, X Band, InGaP HBT MMIC power amp. (chip size: 5mm x 2.6mm [15])

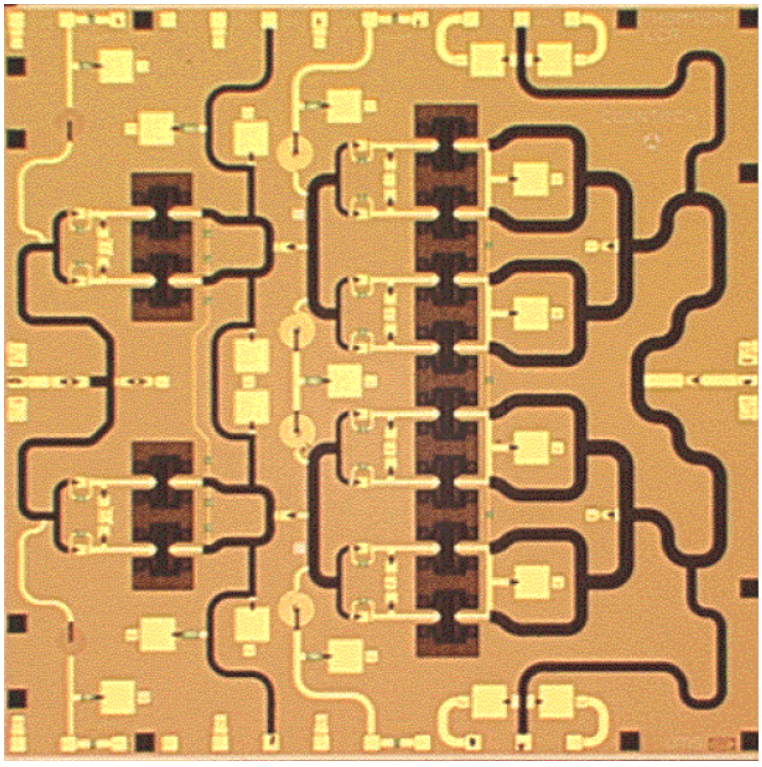


Figure 3.42: 8W, X Band, InGaP HBT MMIC power amp. (chip size: 4.5mm x 4.6mm [16])

Next figures (3.43, 3.44, 3.45 and 3.46) shows graphically the information previously presented in table 3.23:

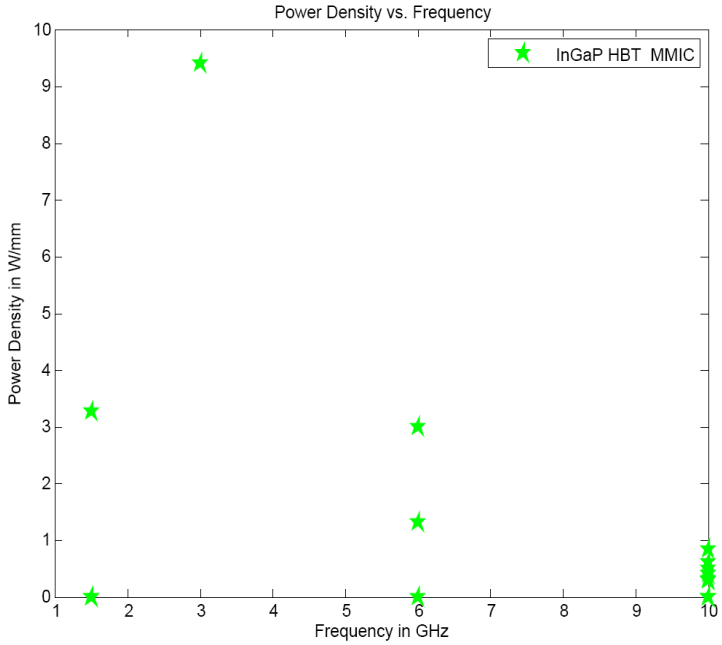


Figure 3.43: InGaP HBT State of Art. Power Density

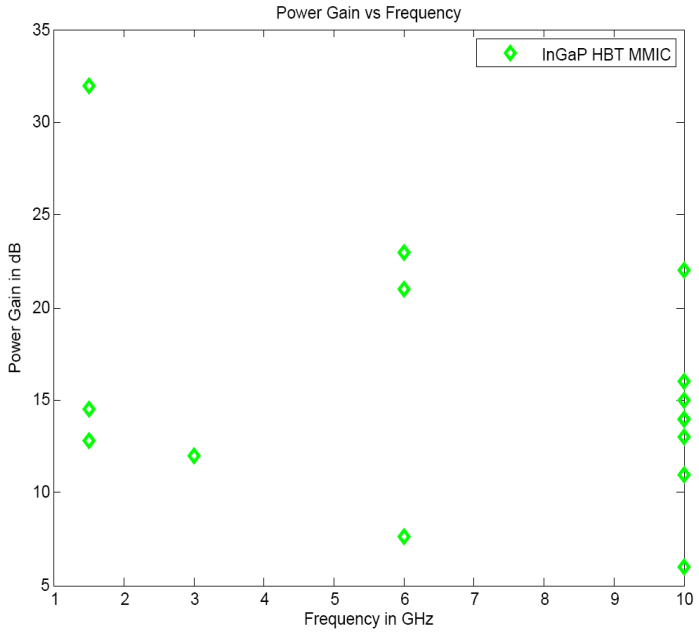


Figure 3.44: InGaP HBT State of Art. Gain

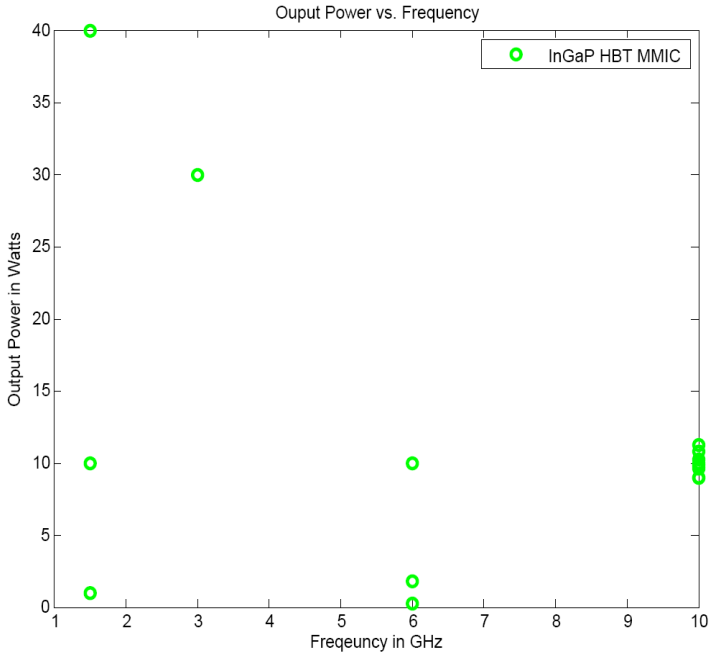


Figure 3.45: InGaP HBT State of Art. Output Power

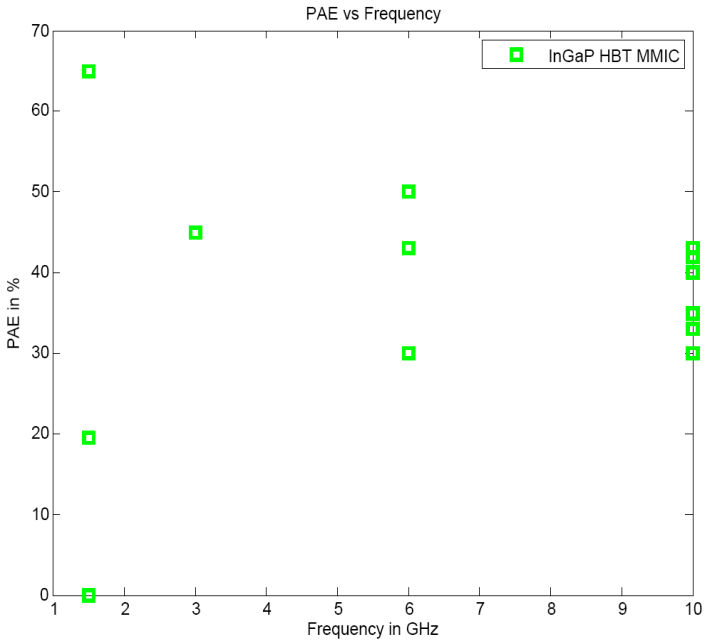


Figure 3.46: InGaP HBT State of Art. PAE

NOTE: In previous Figures those values equal to zero refers to non available data from published works (See Table 3.23).

ACTIVE DEVICE and MMIC COMMERCIAL PRODUCTS

Table 3.24 shows the GaAs HBT foundry process available today.

Process Name	Foundry	Country	f_t GHz	Power Density (W/mm)	Emitter Width (μm)
TQHBT3	Triquint	EUA	40	N/A	3.0
TQBiHEMT	Triquint	EUA	31	N/A	2.0
HO2U-01	WIN Semi	Europe	65	N/A	1.0
HO2U-02	WIN Semi	Europe	35	N/A	2.0
HO2U-32	WIN Semi	Europe	31	N/A	2.0
HO2U-43	WIN Semi	Europe	31	N/A	2.0
HB20S	UMS	Germany/France	12	5	2.0
HB20P(X)	UMS	Germany/France	25	3.5	2.0
HB20M	UMS	Germany/France	30	2.0	2.0
P1	GCS	Taiwan	45	N/A	N/A
P2	GCS	Taiwan	40	N/A	N/A
P5	GCS	Taiwan	32	N/A	N/A
P6	GCS	Taiwan	30	N/A	N/A

Table 3.24: State of Art of commercially available GaAs HBT foundry process

Next table 3.25 shows the most representative state of art commercial products in InGaP technology.

Name	Output Power ($Watts$)	Freq. Band (GHz)	PAE	Gain in dB	Type of Device	Company
HMC407MS8G	1	5-7	28	15	MMIC	Hittite
HMC406MS8G	1	5-6	38	17	MMIC	Hittite
HMC327MS8G	.5	3-4	45	21	MMIC	Hittite
TQP2420	0.5	2.4-2.5	35	31	MMIC	Triquint
MMA701A	0.5	2	N/A	14	MMIC	Aeroflex
AH322	2	0.4-2.7	N/A	13.7	MMIC	Triquint
AP602	4	0.4-2.4	16	15.5	MMIC	Triquint
AP603	7	0.4-2.2	15	11.9	MMIC	Triquint
AP562	8	3.3-3.8	12	11.5	MMIC	Triquint
MMG3006NT1	2	0.4-2.4	N/A	17.5	MMIC	Freescale
SZP-2062	2	2.2-2.7	N/A	11.3	Tr.	RFMD
SKY65014-95	0.1	DC-9	N/A	15	MMIC	Skyworks
SKY65013-92	0.1	Dc-12	N/A	12.5	MMIC	Skyworks
SKY65111-348	2	0.6-1.1	N/A	36	MMIC	Skyworks

Table 3.25: State of Art of InGaP HBT Devices and MMICs - Commercial Products

3.3.5.2 SiGe HBT

ACTIVE DEVICE DESCRIPTION

SiGe is a medium power device due to its low breakdown voltage. However, this limitation is being overcomed continuously each time a new SiGe process is delivered to the market.

The first SiGe HBT was reported in 1987 [186]. Within the next three years, the cutoff frequency of SiGe had reached 5GHz, which clearly exceed the speed obtainable from Si BJTs at that time [187]. Since then, a steady improvement of SiGe HBT high frequency performance have been made.

In general, the vertical structure of a SiGe HBT consist of, from bottom up, a Si substrate, an n+ type Si sub collector, and n-type collector, a p-type strained SiGe base, and a n-type emitter (see Figure 3.47).

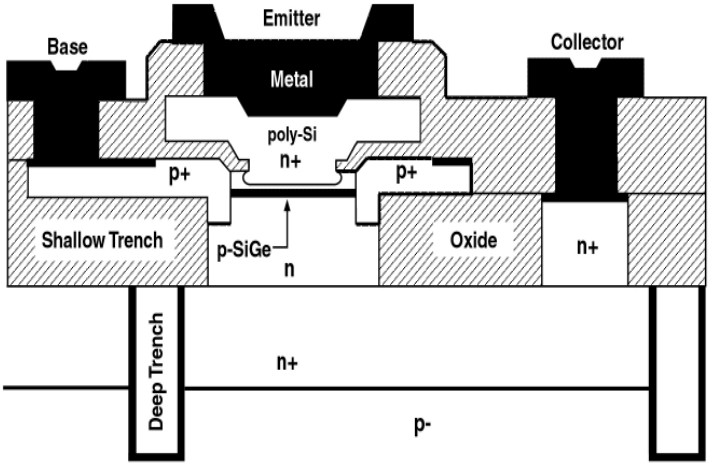


Figure 3.47: Schematic cross section of a SiGe HBT

From the very beginning of SiGe research, two different design philosophies had been developed and investigated, and SiGe based on these two concepts are currently commercially available.

One of te concepts was introduced by IBM nd is frequently called SiGe base HBT [188]. The second concept pioneered by Daimler Benz group, fully exploits the properties of the base emitter junction [189]. The main feature of this device is a base doping considerably exceeding the emitter doping, similar to III-V HBTs. The later device is also known as 'True SiGe HBT'.

Today, the mainstream for microwave applications are the SiGe:C HBT devices [42]. Their success lies in the combination of advanced performance due to bandgap engineering and state of art lithography. In this device the SiGe base is doped with Carbon, which in turn allows to shorten the base width.

Table 3.26 summarizes the state of art in cutoff and maximum frequencies.

f_T	f_{max}
210GHz	89GHz [190]
207GHz	285GHz [191]
170GHz	160GHz [192]

Table 3.26: SiGe HBT Typical Values

ACTIVE DEVICE and MMIC RESEARCH

Silicon Germanium (SiGe) bipolar technology ([193], [194], [195], [196], [19], [197], [198], [199], [200], [201], [202], [203]), is also becoming increasingly important because it offers high integration levels at low cost. Operation at mm-waves is due to high cut-off frequency of SiGe HBT device. Since their breakdown voltages are relatively low, output power exhibited by the power amplifiers is at the lower rank if compared with previous technologies. Nevertheless, SiGe HBT power amplifiers have achieved powers exceeding 0.1W above 60GHz. Even more, if we observe carefully the Johnson theoretical limit for this technology (see Figure 3.2), we could expect some chances to make interesting power amplifiers at X band. Most of the advances in this technology were carried and pushed out by IBM [193], [194] [195].

Different to previous technologies, there are lot off commercial foundries worldwide that offer SiGe. We can mention in EUA: Freescale, Tower Jazz , IBM, Maxim, Atmel,among other. In Europe: IHP (major provider of Infineon and Ericsson), Telefunken, Austria Microsystem, IBM and STMicroelectronics as the principals. In Taiwan: TSMC. In Japan: Hitachi.

From the above among, the best profiled foundries is IBM which leads all the innovation in the digital/analog arena. But the feasibility study perspective there are two foundries that drew our attention: One is IHP (from Germany), that has interesting products in mm wave arena (100GHz and beyond). They are focused in innovative work on SiGe:C (carbon is added) for automotive radar with high breakdown voltages, (above 10V). The other is Tower Jazz in EUA, which worked together with one of the most advanced research team in the subject (Dr. Cressler [42]) funded by NASA to develop roughed SiGe process for space applications. Other foundry to highlight is Telefunken which offer high power (compared to mainstream SiGe power) foundry process.

Next we present the most representative works to unveil the research state of art on SiGe HBT power devices and MMICs.

Output Power $Watts$	Freq. Band	Power Density W/mm^2	Eff. %	Gain in dB	Number of Active Devices	Materials	Foundry	Company or Institution	Year
0.3	Ku	0.72	20	15	3	SiGe Si	N/A	Univ. Korea	2010 [204]
0.1	X	N/A	32	40	2	SiGe Si	IBM	Georgia Tech.	2007 [205]
.85	X	0.18	26	26	4	SiGe Si	IBM	Georgia Tech.	2008 [20]
0.1	X	N/A	25	40	4	SiGe Si	IBM	Georgia Tech.	2007 [17]
0.1	X	0.11	27.4	12	5	SiGe Si	N/A	Univ. Korea	2009 [206]
0.03	V	0.038	20	14	4	SiGe Si	Fraunhofer Inst.	Berlin Univ.	2008 [207]
0.25	C	.14	24.7	12	4	SiGe Si	IHP	Berlin Tech. Inst.	2009 [208]
0.5	C	0.48	28.5	33	4	SiGe Si	Infineon	Bradenburg Univ.	2005 [209]
0.2	C	.125	20	9.7	2	SiGe Si	IHP	Berlin Tech. Inst.	2008 [18]
0.1	Ka	0.55	32	13	2	SiGe Si		California Univ.	2007 [210]
0.06	W	0.1	12.8	17	5	SiGe Si	IBM	California Tech.	2005 [201]
0.13	X	.21	20	9.37	1	SiGe Si	NASA	Winsconsin Univ.	2005 [211]
N/A	C	N/A	N/a	9.3	11	SiGe Si	N/A	Korea Univ.	2006 [212]
0.7	X	0.58	32	9.8	1	SiGe Si	Daimler	Michigan Univ.	2002 [213]
...	...	...	...	...	...	...	...	...	...

Table 3.27: State of Art of SiGe HBT MMIC - Research.

... Output Power $Watts$	... Freq. Band	... Power Density W/mm^2	... Eff. %	... Gain in dB	... Number of Active Devices	... Materials	... Foundry	... Company or Institution	... Year
0.35	Ku	0.29	12	5.5	1	SiGe Si	Daimler	Michigan Univ.	2002 [213]
0.05	Ku	0.76	11.2	15	1	SiGe Si	Infineon	Bradenburg Univ.	2003 [203]
0.016	V	0.005	2.5	6.1	2	SiGe Si	IBM	IBM	2004 [194]
0.1	V	0.13	12.7	18	2	SiGe Si	IBM	IBM	2006 [197]
0.1	K	.099	14	12	4	SiGe Si	Tower Jazz	Georgia Tech.	2006 [19]
0.012	K	N/A	N/A	18	16	SiGe Si	N/A	M/A COM	2005 [196]
0.2	K	N/A	19.7	19	4	SiGe Si		Delf Univ.	2005 [195]
0.078	V	0.034	1	18	6	SiGe Si	IHP	IHP	2007 [214]

Table 3.28: State of Art of SiGe HBT MMIC - Research. Cont.

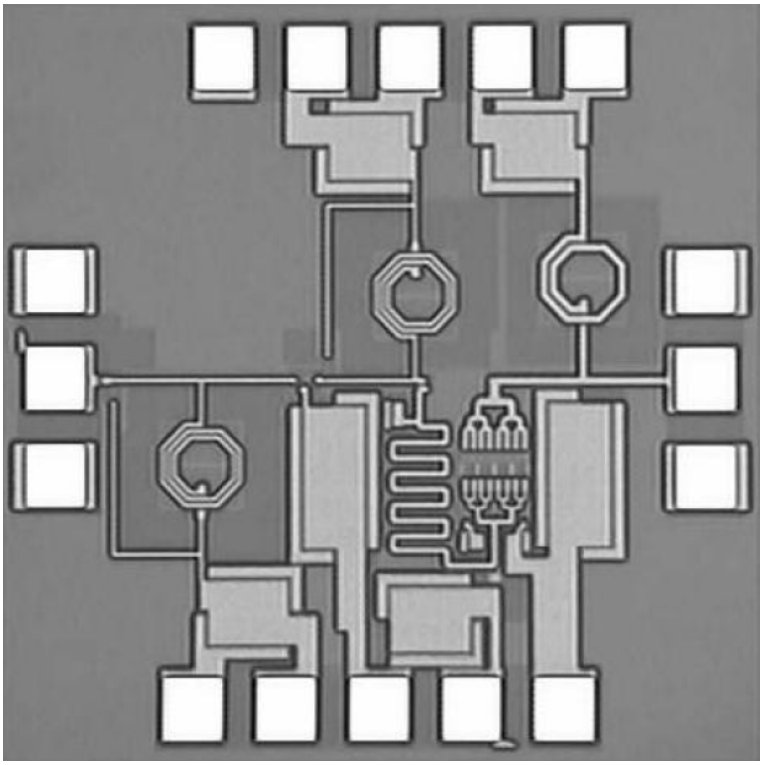


Figure 3.48: 0.1W, X Band, SiGe HBT MMIC power amp. (chip size: 1.1mm x 1.2mm [17])

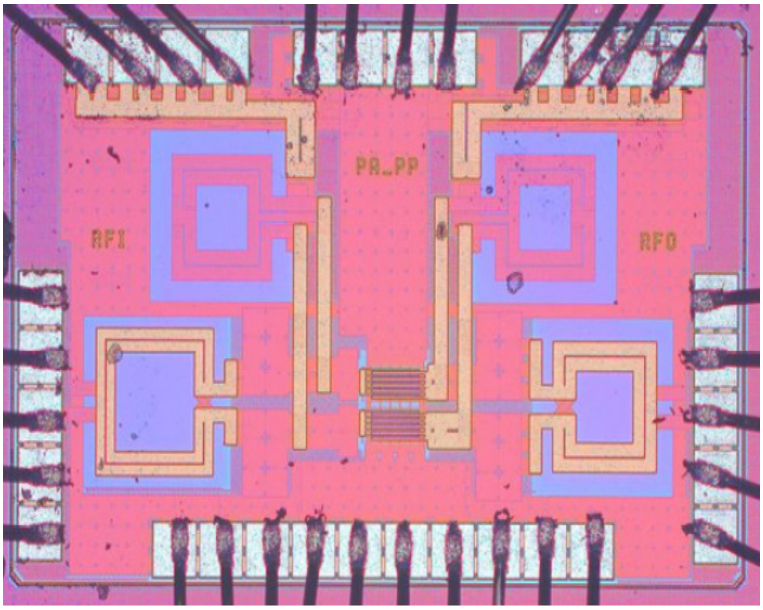


Figure 3.49: 0.2W, C Band, SiGe HBT MMIC power amp. (chip size: 1.6mm x 1.0mm [18])

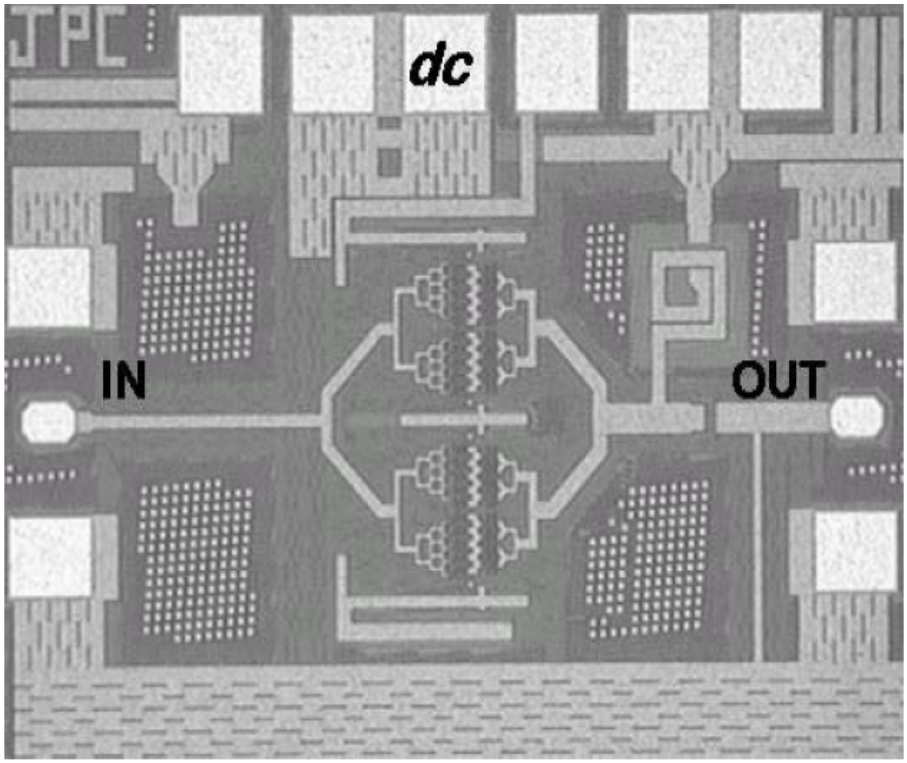


Figure 3.50: 0.1W, K Band, SiGe HBT MMIC power amp. (chip size: 0.85mm x 1.2mm [19])

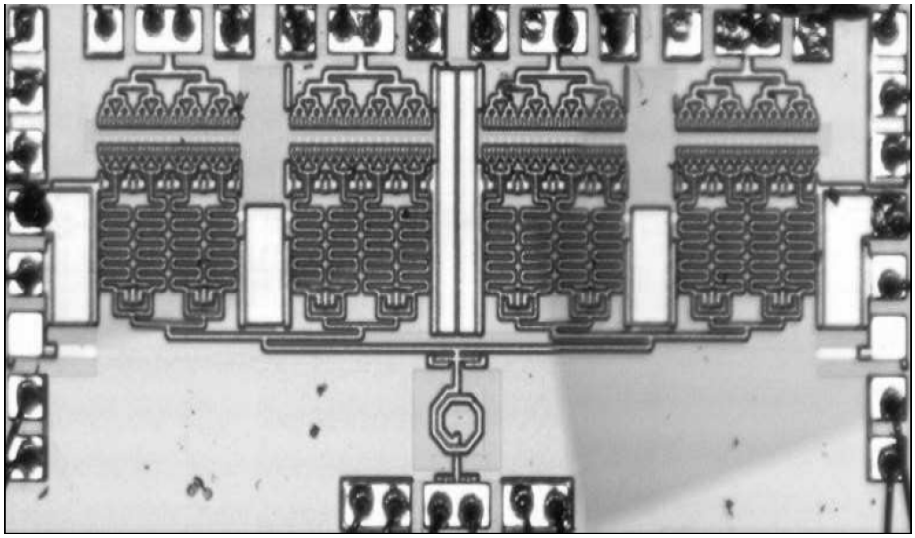


Figure 3.51: 850mW, X Band, SiGe HBT MMIC power amp. (chip size: 1.5mm x 3mm [20])

Next figures (3.52, 3.53, 3.54 and 3.55) shows graphically the information previously presented in tables 3.27 and 3.53:

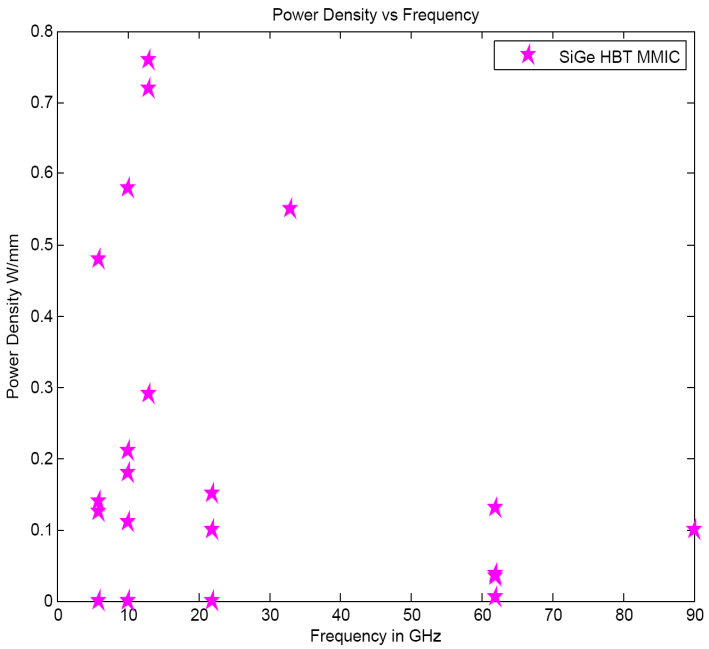


Figure 3.52: SiGe HBT State of Art. Power Density

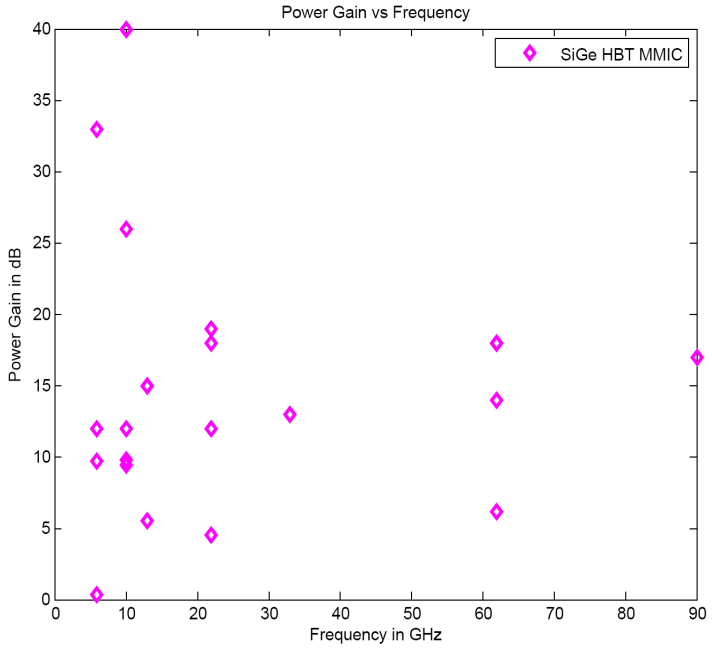


Figure 3.53: SiGe HBT State of Art. Gain

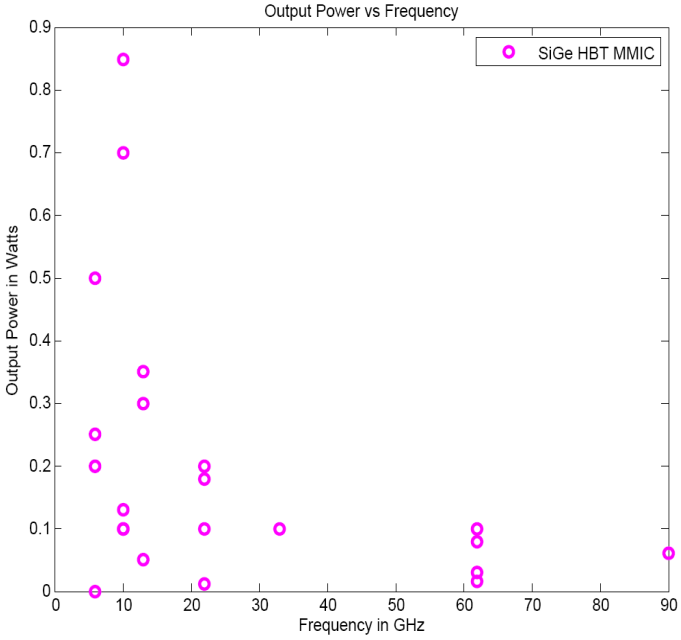


Figure 3.54: SiGe HBT State of Art. Output Power

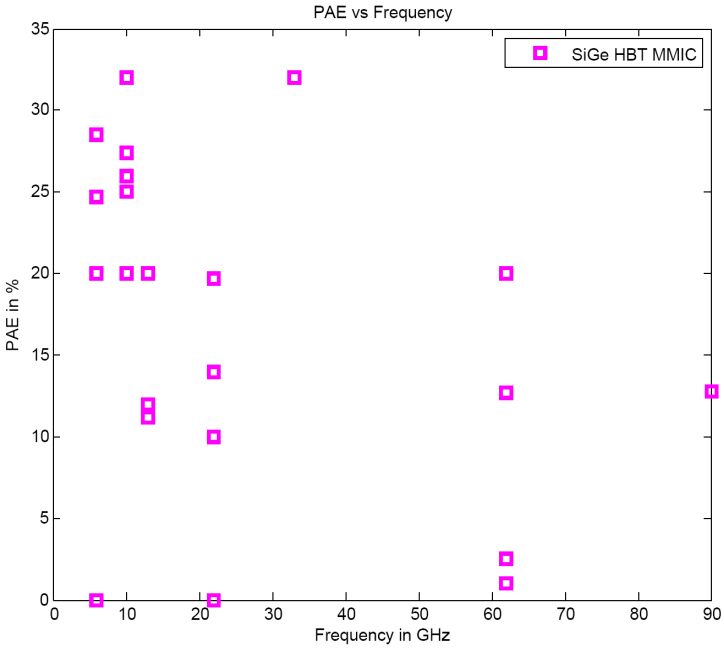


Figure 3.55: SiGe HBT State of Art. PAE

NOTE: In previous Figures those values equal to zero refers to non available data from published works (See Table 3.23).

ACTIVE DEVICE and MMIC COMMERCIAL PRODUCTS

Table 3.29 shows the GaAs HBT foundry process available today.

Process Name	Foundry	Country	f_t GHz	(μm)
6HP	IBM	Europe	47	0.25
7HP	IBM	Europe	120	0.18
8HP	IBM	Europe	200	0.13
8WL	IBM	Europe	103	0.13
0.18Sige	TMSC	Taiwan	65	0.18
0.18SigePA	TMSC	Taiwan	55	0.18
0.35Sige	TMSC	Taiwan	40	0.35
SG25H1	IHP	Germany	180	0.25
SG25H3	IHP	Germany	110	0.25
SG25V	IHP	Germany	95	0.25
SG13S	IHP	Germany	250	0.13
SG13G2	IHP	Germany	300	0.13
HiP6MW	Freescale	EUA	200	0.18
HiP6RF	Freescale	EUA	49	0.18
SBC18PA	TowerJazz	EUA	61	0.35
SBC18H2	TowerJazz	EUA	240	0.18
SBC18H3	TowerJazz	EUA	200	0.13
SiGe2PW Power	Telefunken	Germany	33	0.8
SiGe2RF Power	Telefunken	Germany	50	0.8
BiCMOSMW	ST Microelec.	Europe		
S35D4M5	Austria Microsyst.	Europe		
SGST-35	Maxim	EUA	N/A	N/A
GST-4P	Maxim	EUA	N/A	N/A
B200M00	Hitachi	Japan	210	0.18
B140M00	Hitachi	Japan	173	0.18

Table 3.29: State of Art of commercially available SiGe HBT foundry process

Next table3.30 shows the most representative state of art commercial products in SiGe technology.

Name	Output Power ($Watts$)	Freq. Band (GHz)	PAE	Gain in dB	Type of Device	Company
HMC474SC70	0.006	DC-6	N/A	15	MMIC	Hittite
HMC476MP86	0.016	DC-6	N/A	20	MMIC	Hittite
SGA-4300	0.025	DC-4.5	N/A	14.6	MMIC	RFMD
SAMP 7710	0.025	DC-3.5	N/A	14	MMIC	RFMD

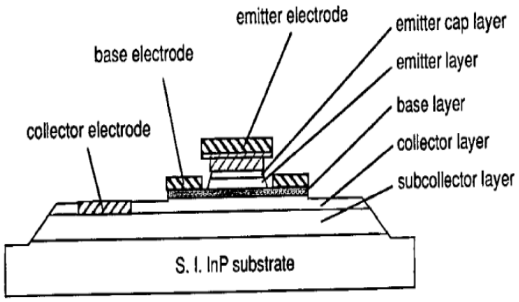
Table 3.30: State of Art of SiGe HBT Devices and MMICs - Commercial Products

3.3.5.3 InP HBT

Recent attention is also focused to InP HBT, which have much higher cut off frequencies than their GaAs counterparts. It enables the construction of power MMICS [215], [216], [217], [218], [219], [220], [221], [222], [223] operating at even 175GHz. It should be mentioned that most of the reported designs employ double heterojunction (DHBT) to boost the power handling capability. Using this scheme reduces device losses and improves breakdown voltages while sustaining high cut off frequencies. It is interesting to observe that these devices exhibit very high power densities event at high frequencies, generally outperforming all other devices including InP HEMTs. However, the output power remains limited due to small device periphery.

Today there are companies that offer foundry services in for InP HBT technology. The most important are: Triquint, Vitesse, GCS, OMMIC, Northrop Grumman (defense) and HRL Laboratories (defense) among others.

Figure 3.56 shows the cross section layers of an InP based HBT:



layer	composition	thickness (nm)	carrier density (cm^{-3})	doping
emitter cap	n^+ -InGaAs	30	$4x10^{19}$	Si
	n^+ -InP	20	$2x10^{19}$	Si
emitter	n^- -InP	50	$3x10^{17}$	Si
spacer	un -InGaAs	5	-	-
base	p^+ -InGaAs	50	$3x10^{19}$	C
collector	n^- -InGaAs	300-500	$2x10^{16}$	Si
subcollector	n^+ -InP	400	$3x10^{19}$	Si

Figure 3.56: InP HBT Cross section layers.

Figure 3.56 shows other version of cross section layers of an InP based HBT developed in HRL Laboratories:

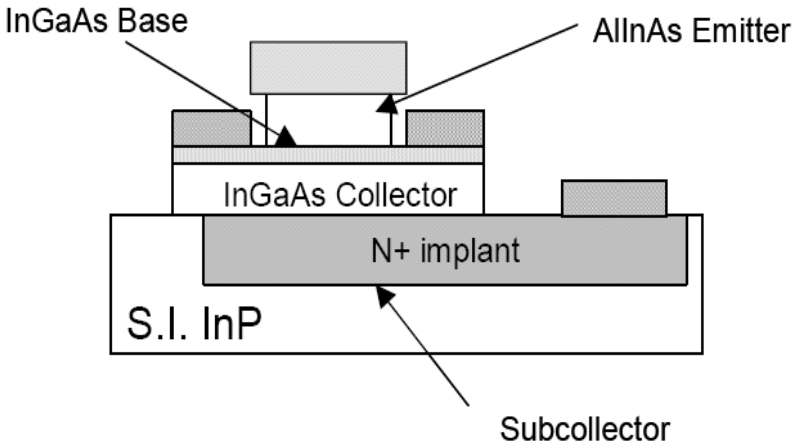


Figure 3.57: InP HBT Cross section layers.([21])

Typical values for InP HBTs devices are showed below in table 3.31:

Type	f_T	f_{max}
InP/InGaAs DHBT	300	238 [224]
InP/InGaAs DHBT	209	300 [225]
InP/InGaSb DHBT	270	300 [226]
InP/InGaSb DHBT	305	230 [226]

Table 3.31: InP HBT Typical Values

SUMMARY.

- The mainstream devices for power GaAs HBT are represented by GaInP emitter based HBT. AlGaAs based no longer exist as a state of art foundry process. In China however, one foundry still offer this product.
- As happen with other technologies, to reach the multi watt applications many active devices must be integrated in a chip.
- The state of art show a frequency limit for this technology at X band (for power applications).
- Most of the innovative X band works are done today in Europe by UMS Foundry, in cooperation with space companies (government and private).
- InGaP HBT is more dense in terms of power/area but thermal handling aspects are an issue.
- Commercial products are available in the InGaP technology, however at X band few products were found and with lower power than required.
- There are several companies that offer commercial foundry service for SiGe and InGap.
- SiGe HBT is still confined in the state of art to low power and medium applications but, the power capabilities shall studied carefully from the current feasibility study perspective.
- Commercial product in SiGe verifies the power limitation up to date of this technology.
- InP HBT falls out of scope of this feasibility study.

Table 3.32 shows a survey of current advanced bipolar devices an their technological aspects that allowed bipolar devices to compete in microwave applications:

Devices	Main Features
Silicon Bipolar Technology BJTs * Advanced fabrication techniques are allowing devices with $f_T \approx 25GHz$	* Self Aligned Emitter Base. * Trench Isolation to avoid cross-talks. Sidewall Contacts. Polysilicon is used to contact the base. * Polysilicon emitter contact. Provides low recombination at the contact and suppresses base injection into the emitter.
Silicon Based HBTs. * Si/SiGe HBTS have shown remarkable promise. Cutoff frequencies approaching 100GHz have been demonstrated	Si can be combined with * amorphous silicon ($E_g = 1.5eV$) * SiC ($E_g = 2.2eV$) * polysilicon ($E_g = 1.5eV$) * SiGe, is the mostpromising combination since can be fabricated by epitaxial growth
AlGaAs and InGaP HBTs * $f_T \approx 100GHz$ has been demonstrated.	* Excellent quality of interface allows fabrication of high quality HBTs. * Devices can be monolithically integrated with optoelectronic devices.
InGaAs/InAlAs and InGaAs/InP HBTs * $f_T \approx 175GHz$ has been achieved	* Exists configurations of InGaAs that are lattice matched to InP and InAlAs. * High quality HBTs can be produced and integrated with opticla devices.

Table 3.32: Survey of Advanced Bipolar Devices

3.4 State of Art Survey and General Conclusions

Nexts figures shows a comparative view of the technologies under study in terms of: power density, power gain, output power and power added efficiency.

3.4.1 State of Art Survey

3.4.1.1 Active Devices Performance Comparisons- Power Density vs Frequency

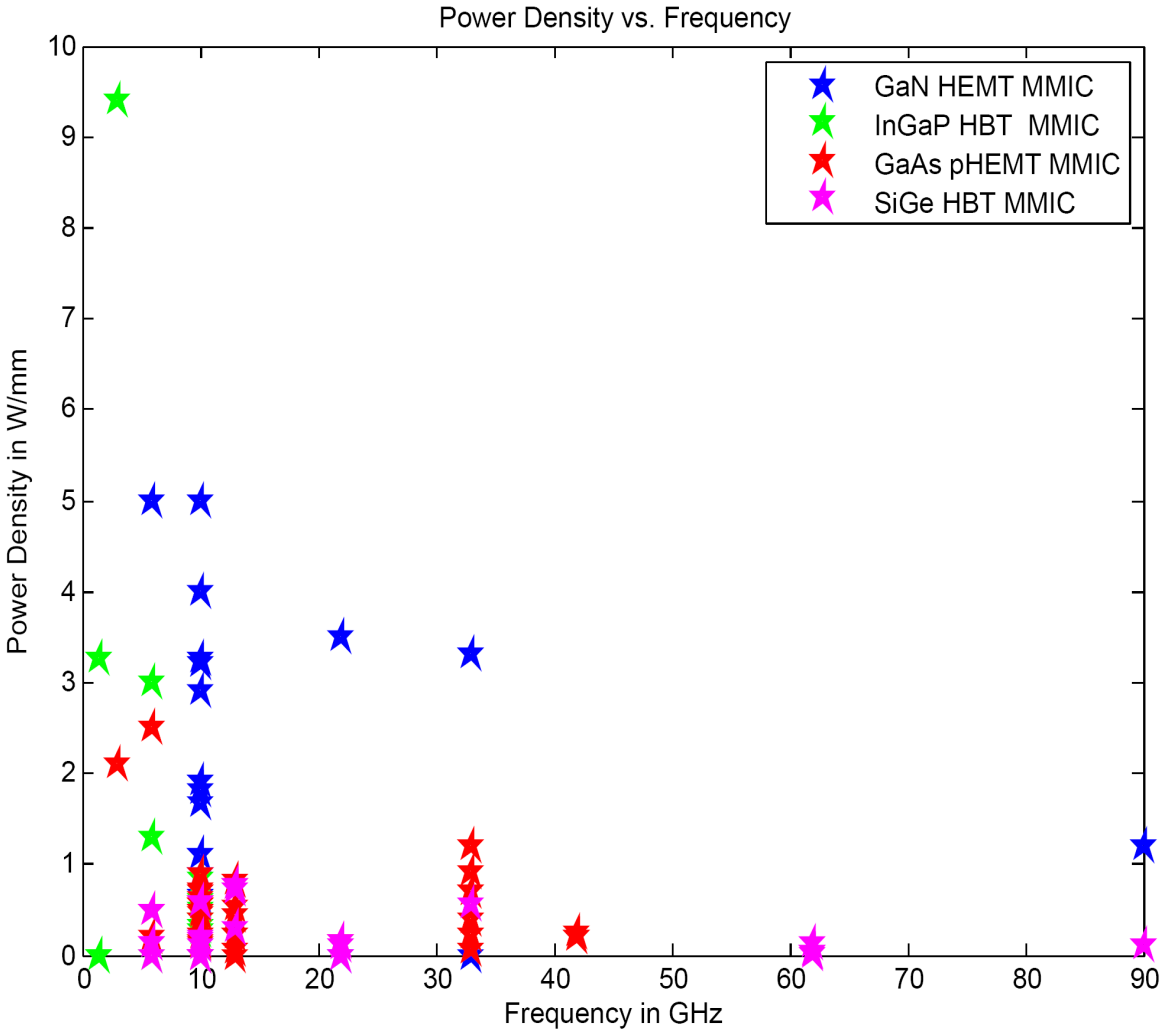


Figure 3.58: MMICs State of Art- Power Density

3.4.1.2 Active Devices Performance Comparisons- Power Gain vs Frequency

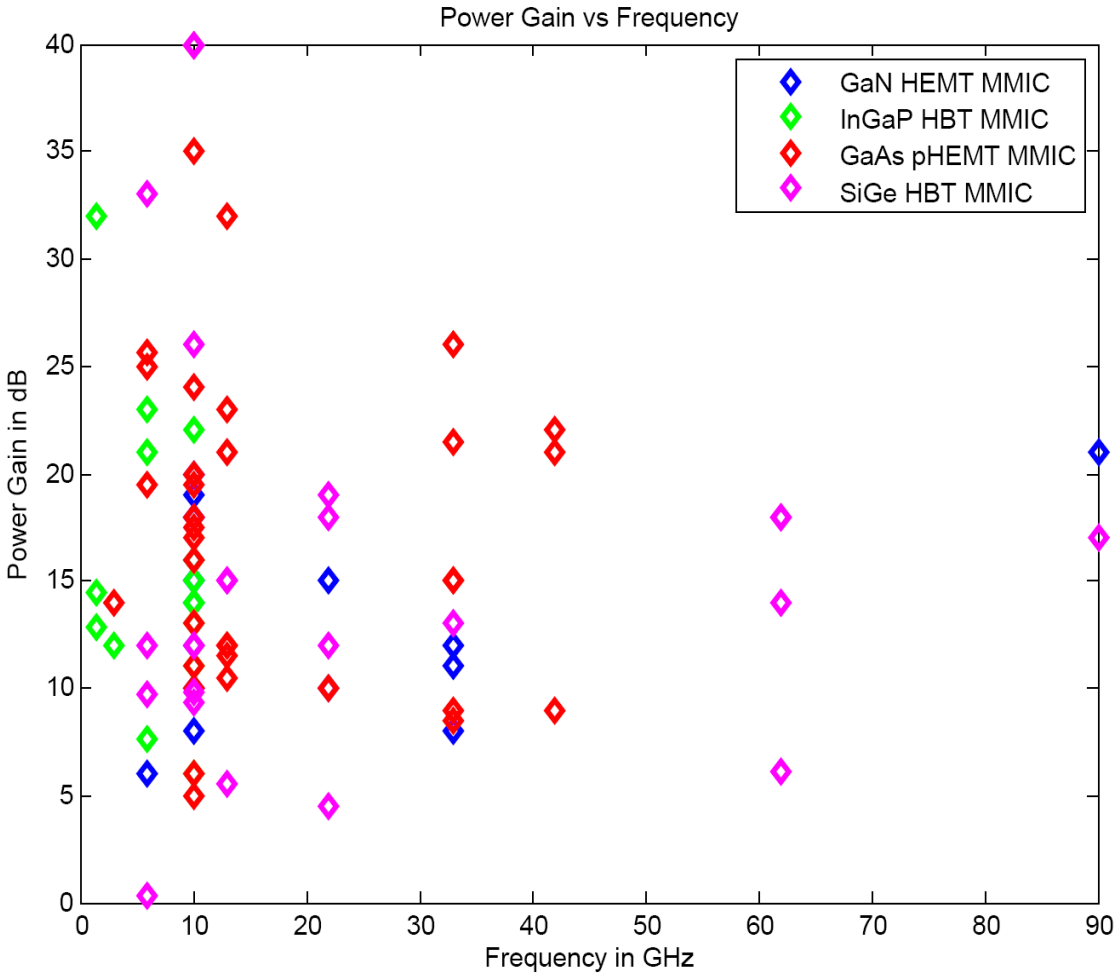


Figure 3.59: MMICs State of Art. Power Gain

3.4.1.3 Active Devices Performance Comparisons - Output Power vs Frequency

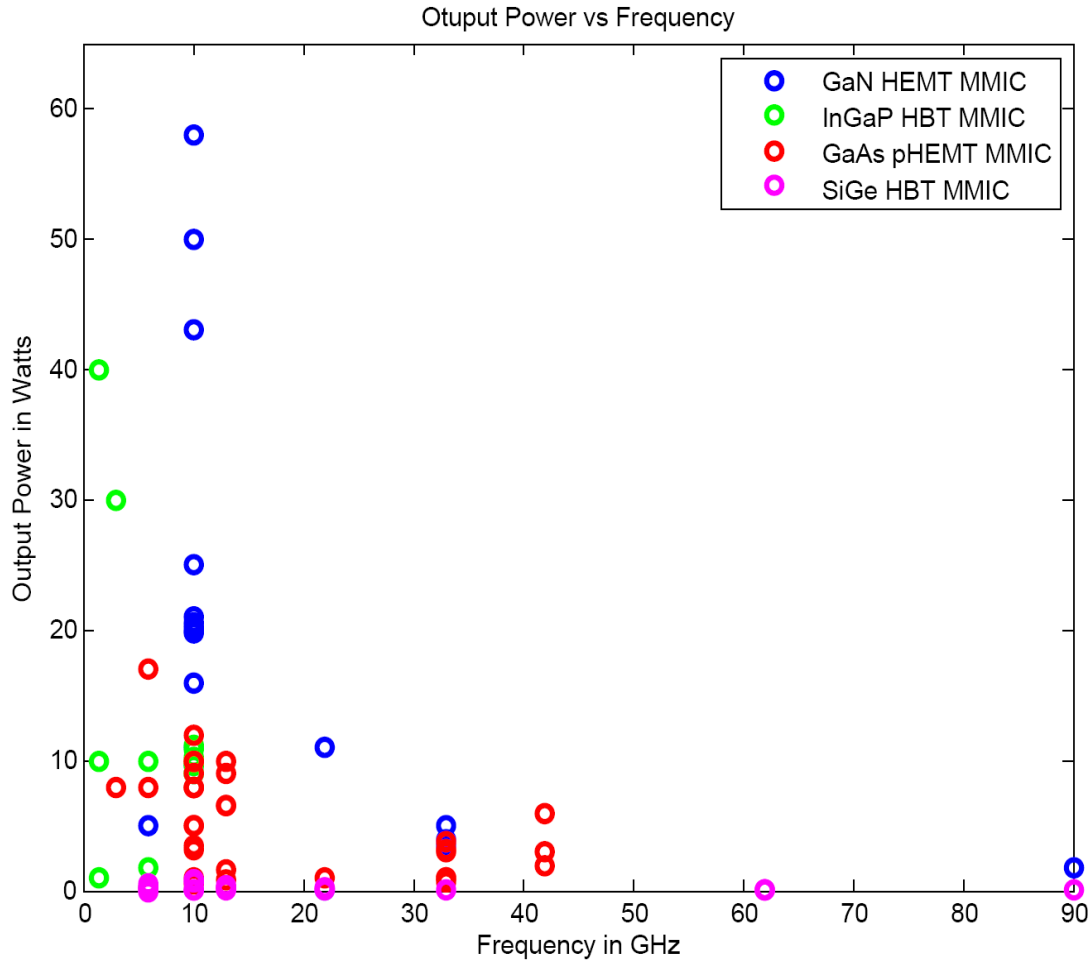


Figure 3.60: MMICs State of Art. Output Power

3.4.1.4 Active Devices Performance Comparisons - PAE vs Frequency

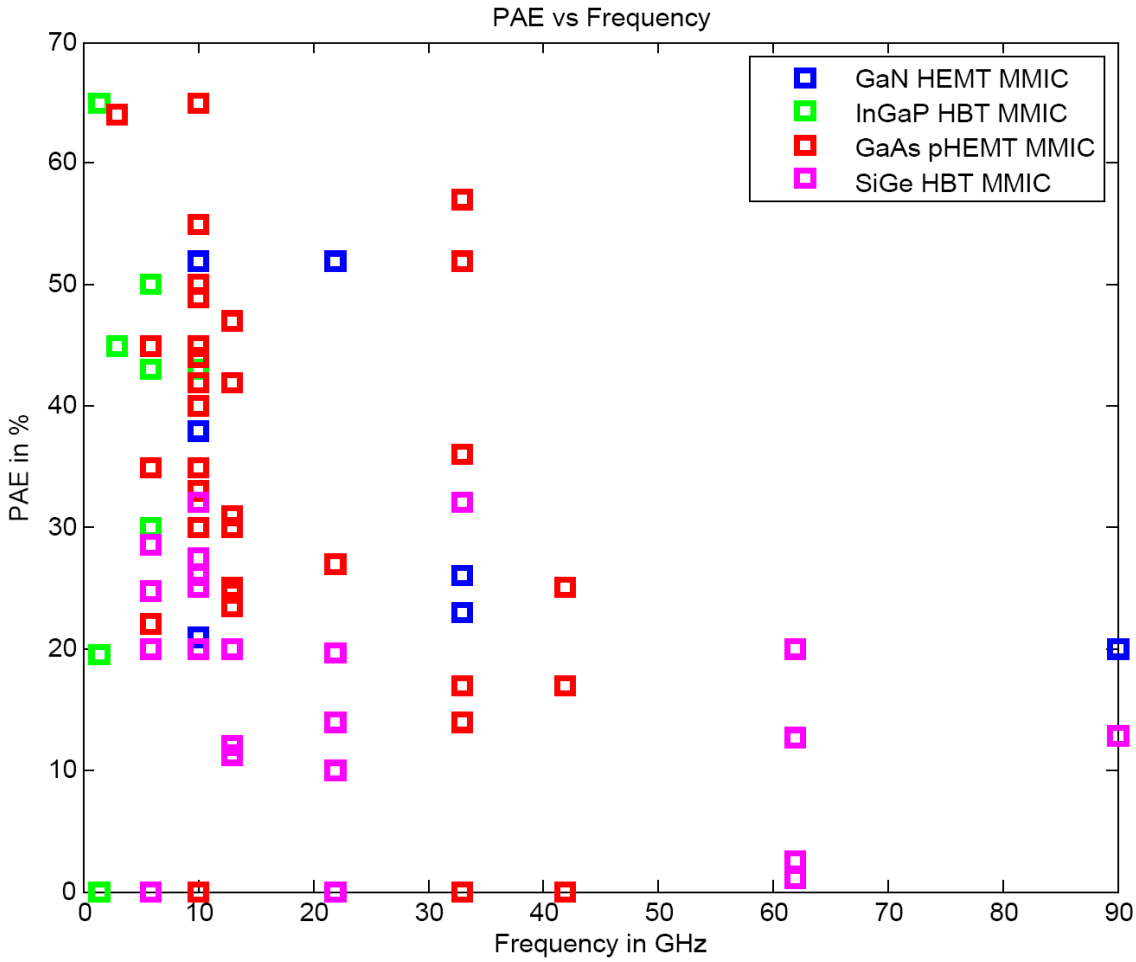


Figure 3.61: MMICs State of Art. PAE

3.4.2 General Conclusions

For GaAs based devices:

- GaAs based pHEMTs and HBTs are the most established technologies for application of the feasibility study in course. Its maturity state respect to other technologies is a key factor to be taken into account.
- InGap HBT and AlGaAs/InGaAs pHEMT are the state of art power devices in GaAs substrates.
- InGap HBT and AlGaAs/InGaAs pHEMT state of art MMICs meet the requirements for this feasibility study.

- Commercial related products confirm the above mentioned.
- If higher frequencies were required (for example K,Ku,Ka bands for satellite comms.) AlGaAs/InGaAs pHEMT has a clear performance advantage over InGaP HBT.
- Today, there are foundry companies that offer services either for InGap HBTs or AlGaAs/InGaAs pHEMTs, allowing third party (us) MMICs manufacturing.

For SiC based devices:

- SiC based HEMTs are to date the most powerful microwave active device achieving the highest power densities and breakdown voltages.
- AlGaN/GaN on SiC substrate HEMT is the state of art active device in this technology.
- GaN on SiC HEMTs active device are quite new in the industry (10 years), then reliability and manufacturing costs are still open issues.
- AlGaN/GaN on SiC HEMTs state of art MMICs meet the requirements for this feasibility study.
- Commercial related products confirm the above mentioned.
- If higher frequencies were required (for example K,Ku,Ka bands for satellite comms.) AlGaAs/InGaAs pHEMT has a clear performance advantage over the AlGaN/GaN on SiC HEMT.
- To date, there are foundry companies that offer services for AlGaN/GaN on SiC HEMTs allowing third party (us) MMICs manufacturing.

For SiGe based devices:

- SiGe technologies far exceed the frequency requirements for the current feasibility study. Its power handling is less than required although presents unexplored and potential possibilities at X band.
- SiGe is commercial products at X band are far below in terms of power.
- To date, there are foundry companies that offer services for SiGe on Si HBTs allowing third party (us) MMICs manufacturing.

For InP based devices:

- InP HBTs and pHEMTs devices meet the highest frequency requirements up to date.
- InP HBTs and pHEMTs can not meet the power specifications for the current feasibility study.
- InP HBTs and pHEMTs are quite novel technologies.
- To date, there are foundry companies that offer services either for InP HBTs or pHEMTs, allowing third party (us) MMICs manufacturing.

For all devices:

- In this chapter we found at least four groups of technologies that potentially fits the feasibility study requirements. They are: GaAs pHEMT, SiC HEMT, Si HBT and GaAs HBT.
- Their respective active devices are: AlGaAs/InGaAs on GaAs pHEMT, AlGaN/GaN on SiC HEMT, SiGe on Si HBT and InGaP on GaAs HBT.
- All the above technologies and devices have available commercial foundry services up to date.
- We recognize for decision making on the semiconductor process selection the following primary aspects: Availability, Reliability, Cost, Power and Frequency.
- We recognize for decision making on the semiconductor process selection the following secondary aspects: Efficiency, Voltage, Gain and Linearity.
- At the end of the feasibility study a weighted function of the above aspects shall be presented for decision making.

Chapter 4

Electronic Design Automation (EDA) Tools Evaluation (Third Deliverable Document)

This Chapter deals with today available EDA tools needed for design microwave power transistors and MMICs. An overview of main characteristics with the aim to understand the most important aspects is presented below.
The description is based on current available tools at both laboratories, LAPSyC and GISEE.
The summary roughly describes what are the main aspects to be taken into account prior to the project start up in order to get the best tool that guarantee a project success.

4.1 Introduction

The Electronic Design Automation (EDA) softwares have become today in a key part in the full design cycle of a modern integrated circuit design either, at radio frequencies or microwaves frequencies.
Today, the major part of design cycle relies on the simulation results of the software tools. They in turn, are based on the confidence reached by the physical models, mostly achieved in the last decade [227]. Today models can represent with high fidelity a widespread set of parameters and physical phenomenas of the active and passive devices components such as, bias operation variation, thermal variability, non linear current sources, non linear capacitances, breakdown voltage effect, vknee effect, and so on. When better is the model, closer are the simulation results to the measurement results of certain circuit, higher the probability of first pass design success and better the performance of the simulation tools.
From the project's perspective, the EDA tool is used to design the schematic circuit, simulate its performance, design the layout circuit, simulate its performance, make a circuit optimization if required (if electromagnetic simulation is available much better), and finally, run the design rules check to validate that the layout design is according to the manufacturer physical design rules.
The design steps mentioned previously are the usual steps in a EDA tool design flow.
In today microwave market there are basically three main EDA tools that can handle analogous integrated circuit designs at microwaves frequencies as those required by CONAE. They are: Microwave Office from Applied Wave Research [228], Advanced Design System from Agilent (ADS) [229] and Cadence Design Systems [230] among others.
Our laboratory have already installed and is currently working with Agilent ADS and Cadence Design System. Also have human resources with design experience in both softwares.
For the mentioned above we will only describe the main characteristics for the available tools (ADS & Cadence).
There are no important differences between Cadence and ADS although, each tool has its specific profile. Below we present brief description of the main characteristic of each EDA tools separately.

4.2 Cadence Design System

The Cadence tools for RF design provides a comprehensive array of capabilities for electrical and statistical analysis, verification, and optimization of analog/mixed-signal designs, including the interfaces to many industry-standard simulators.

The specific design tool of the Cadence design environment is called Virtuoso Analog Design Environment, his outstanding features are described in the next list:

- *Circuit Design:* Selectively automating non-critical aspects of RF design allows project designer to focus on precision-crafting their designs. Cadence circuit design solutions enable fast and accurate

entry of design concepts, which includes managing design intent in a way that flows naturally in the schematic. Using this advanced, parasitic-aware environment, designers can visualize and understand the many interdependencies of an analog, RF, or mixed-signal design, and can create and verify selected passive components.

- *System Level Simulation:* It is a complete flow-from system-level design to post-layout verification-that integrates circuit simulation with RF system-level and mixed-signal baseband designs. Cadence technology offers flexible system-level simulation for RF and digital blocks, enabling the verification of RF blocks within a digital environment. Co-simulation capability with data-flow simulators allows system designers to explore the effects of non-ideal circuits on system architecture.

- *Layout Design:* layout solutions automate and accelerate custom block authoring. They provide advanced features for device generation and editing, block floor planning, automatic placement, and interactive routing.

- *Parasitics Extraction:* After layout, RF designers must go back into the design to locate parasitics and perform another round of simulation to determine where parasitic effects will cause problems. Cadence solutions for parasitic extraction make it easy to get a holistic view of all the parasitic effects in a design, and then quickly correct them by flagging violations of design rules in real time.

- *Manufacturability signoff:* At today's advanced technology nodes, RF design software must account for the challenges of smaller transistors and wires, as well as the data capacity and complexity challenges of denser, more intricate chips. Cadence solutions for manufacturability take the knowledge of creating the mask and how the chip is going to be manufactured and bring it back into the design phase. This helps designers compensate for physical effects while providing a reliable way to achieve manufacturing signoff before tapeout.

4.2.1 Installation and Licenses Status at GISEE

To date, the GISEE has academic licenses of Cadence Virtuoso IC5 version. The software is running on stand alone personal computers (Linux) and on a IBM server platform (Linux).

4.3 Agilent ADS

The main features of the ADS soft are described in the next list:

- *Circuit Design:* ADS deliver a schematic design tool with several simulation capabilities (transient, statistical, harmonic balance and time domain, among others). This tool allows the design and simulation of MMICs circuits based on process design kit provided by the semiconductor manufacturers.

- *System Level Simulation:* The most featured system level simulation is the Ptolemy co-simulation which allows the evaluation of a RF block design in a signal processing (DSP) environment. This very useful tool is used to evaluate the effects of analog designs in the overall system structure in a very efficient way.
- *Layout Design:* Layout bundle includes the most needed design capabilities to support the full RF board design flow ranging from schematic capture, linear simulation with fast, agile tuning, optimization, statistical design for highly productive layout capability.
- *Parasitics Extraction:* Not available.
- *Planar EM and 3D EM simulation:* Add to software the ability to verify, prior to fabrication, that a MMIC meets all specifications in its final package, using seamlessly integrated Planar EM and 3D-EM tools.
- *X parameters models:* One of the advantages of ADS over Cadence environment is the capability of ADS to work with models extracted directly form simple measurement setups.The X-parameters, extracted with non linear vector analyzer measurements, are a mathematical superset of S-parameters and are used for characterizing the amplitudes & relative phase of harmonics generated by nonlinear components under large input power levels.

4.3.1 Installation and Licenses Status at LAPSyC

To date, the LAPSyC has academic licenses of ADS 2011A version, this license includes a fee for an on-line technical support to keep the system working on. The software is running on stand alone personal computers (Windows and Linux) and on a IBM server platform (Windows and Linux). The Linux feature is very important since some manufacturer only provide PDKs on Linux version.

4.4 Summary

There are not substantial differences between both tools. The selection for one or other shall be based mainly at first, on the availability of semiconductor device models (Process Design Kits (PDKs)) since this tool conditions the overall design flow.
Below we describe the most important features of both softwares from the current project's perspective:

- Cadence Virtuoso features: a leading RF EDA tool with the most innovative successful technologies, including Harmonic Balance, Circuit Envelope and System Level Simulation.
- There are in GISEE lab human resources able to design microwave circuits with Cadence tools.

- There are human resources trained to support the functioning of Virtuoso tool at GISEE.
- ADS features: the leading RF EDA tool with the most innovative and commercially successful technologies, including Harmonic Balance, Circuit Envelope, Transient Convolution, Agilent Ptolemy, X-parameter, Momentum and 3D EM simulators (including both FEM and FDTD solvers).
- ADS allows measurement based models such as: S2P, P2D and X parameters. The later is the most powerful and is described in next Chapter.
-
- There are in LAPSyC lab human resources able to design microwave circuits with ADS tools.
- There are human resources trained to support the functioning of ADS tool at LAPSyC.

Final remarks, during this feasibility stage we described the available EDA tools needed for the project completion. However, is not clear what is best a priori, since there are many features that requires a joint evaluation prior to make a decision on what tool must be used. Anyway, we identified some features of vital importance for the project success. One is how the design software interacts with measurement models (defines the instruments characteristics), other is the capability of EM simulation (circuit optimization and packaging analysis), finally the system level capabilities or co simulation RF-DSP (full circuit evaluation in realistic conditions). Since Cadence and ADS can be complemented one each other through the Golden Gate software [231] getting in that way the best of both at same time, we recommend a careful study of the mentioned EDA tools prior to project start to balance properly the required features.

Chapter 5

Passive and Active Devices Modeling and Measurements for Characterization (Third Deliverable Document)

This chapter presents an overview of both, physical models provided by the foundries and the behavioral (black box) models currently used for the characterization of passive and active devices. Also describe the measurement techniques and different setups of laboratory instruments used to characterize the device with some behavioral model further used.

The main objective of this chapter is to roughly describe the benefits and drawbacks of physical and behavioral models, in order to have a better background during the evaluation of the MMIC foundry process trade offs.

The chapter is divided as follows. First, the device's physical models provided by foundries are reviewed, covering the main aspects involved in this study. Second, the behavioral models used to characterize devices and systems are covered with emphasis on available EDA Tools. After that, the measurement techniques and the laboratory instruments setups required to characterize are reviewed. Finally, we present a brief discussion and comparative tables focused on the decision making stage.

5.1 Introduction

Today a big percentage of the full microwave MMIC design flow is performed inside the simulation tools environment. The main motivation of this trend is related to the increasing availability of complex models for the passives or the active devices. So, careful attention must be payed to the physical models provided by the foundries and in turn, to the behavioral models that would be used to characterize the designed device or module with the laboratory characterization measurements.
Among the physical models we only describe those provided by semiconductor process manufacturers. On the other hand, among the behavioral models possibilities we deal only with those models that can be implemented in the simulation tools.
From the perspective of this feasibility study we classify the physical models as those provided by the foundry and behavioral models as those that must be delivered by a laboratory as part of a device characterization result.
Physical models represents the more detailed description possible of a certain device and can not be extracted today at our laboratories due to the lack of instruments and specialists. On the other hand, behavioral models can be provided today using our laboratory capabilities despite that for better behavioral models, new instruments and accessories would be required.
In next sections we present a detailed description of the physical and behavioral models involved in this feasibility study.

5.2 Passive Devices Modeling

Passive elements can be represented by linear and nonlinear models. Although strange, passive components can also have a nonlinear behavior, as for example the coaxial transmission lines at the output of a base station which produce inter modulation between frequency carriers at high power range. Due to the operating power range this feasibility considers the linear modeling of passive elements only. The main technique for modeling the passive is by means of S parameters measurement realized with a vector network analyzer instrument and the further representation of this measurements in a S parameters table. This model is reviewed with more details in next sections.
From the current perspective, one of the main concerns is related to the error correction techniques [232] applied to the S parameters measurement setup [233], [234]. That is addressed to obtain more accurate models considering the systematic measurement errors caused by the non infinite directivity of the directional couplers on which VNA instruments are based.

5.3 Active Devices Modeling

The active models are one of the most important design aspects (among other critical issues) to be take into account in current feasibility study. Specially, a good nonlinear model is critical for a reasonable

design success allowing low number of prototype iterations (and in some cases a first pass design success). The quality of the model has a strong influence on the human resources and foundry runs costs.

Active models are intimately related to the measurement setups used. They are divided basically in two major groups of particular interest: *C*ompact Models (Physical) and *M*easurement-Based Models (Behavioral). As a rough classification we can say that the first ones are those provided by foundry companies and the second ones are those models obtained when a device is characterized in the laboratory, although the limits for this classification are still not well defined.
Following we present a rough description of both classes of models focusing on the design benefits provided by them and the instrument setups required to derive them.

5.3.1 Compact (Physical) Models

Compact models are typically defined internally by a set of analytical equations that allows to describe the intricate behavior being modeled. A parameter model set connect the internal behavior of the model to its external use by the *m*odel maker and the simulator. While extracting these parameters can be very difficult, developing the underlying equations is even more cumbersome. These models deserve the effort however, because they can provide ways to optimize the device design if the underlying model is physically correct.
Next, among many models available in the semiconductor industry, we will describe only those provided by the foundries pre selected for this feasibility study.

5.3.1.1 Materka (Triquint) [235]

The modified Materka model is a schematic based model. Its current source (and therefore output conductance) is a nonlinear function of terminal voltages, a result of fitting to pulsed I-V data. All other resistances and capacitances are fixed at values obtained from S parameter at the quiescent bias.
Figures 5.1 and 5.2 shows the large and small signal equivalent circuits for Materka model.

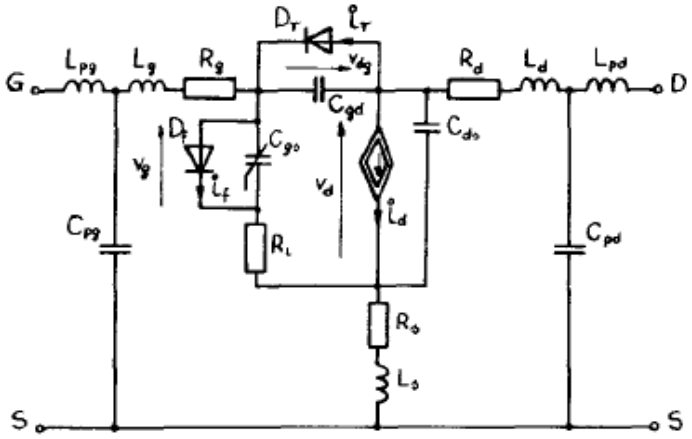


Figure 5.1: Materka large signal equivalent schematic circuit

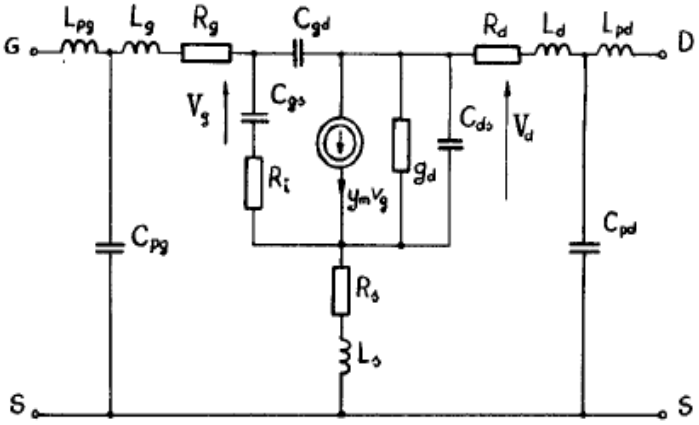


Figure 5.2: Materka small signal equivalent schematic circuit

The modified Materka model is fitted to the first quadrant pulsed I-V, gate source forward conduction, gate-drain breakdown, and small signal parameter data.S parameter and pulsed I-V data are collected only for the intended quiescent operating bias point. As a result, the Materka model should be used only at that quiescent point, and a separate Materka model must be fitted if another bias point is needed. The Materka model does not provide accurate DC or RF simulation at another operating than the modeled quiescent point.

Being fitted at only one bias point, the modified Materka model can be matched very closely to its small S parameter data. Agreement with the linear small-signal model is within approximately 5% across frequency, and 2% matching is typical.

5.3.1.2 TOM3 (Triquint, RFMD) [236]

TOM-3 model is a charge-based model, and lacks of a conventional equivalent-circuit schematic. It may be re-biased over a reasonable portion of the first quadrant of its I-V characteristics (if Id not to exceed Idss (saturation)), and therefore provides reasonable DC simulation and self-bias solutions.
Figure 5.3 the equivalent circuits for TOM3 model.

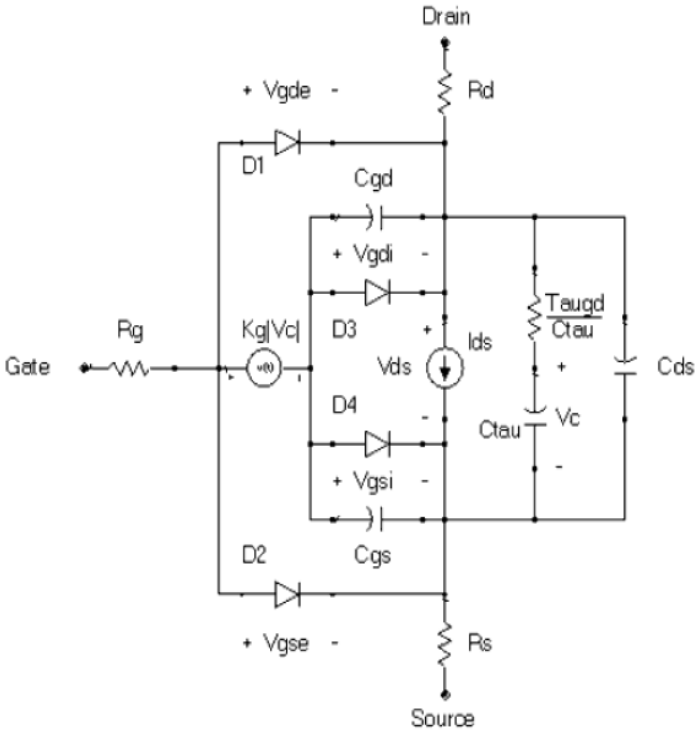


Figure 5.3: TOM3 equivalent schematic circuit

TOM-3 model is fitted, using internally-developed software, to DC I-V (first-quadrant drain characteristics and DC IV of the gate-source diode) and small-signal S-parameters. The S-parameter data is collected at each individual DC bias point in the first quadrant, and the S-parameter fit is balanced over this range of bias.TOM-3 model may be re-biased over this fitting range to simulate both DC and RF performance. TOM-3 model should not, however, be biased above Idss. TOM-3 model was originally developed as a general-purpose simulation model for low frequency MESFETs used in mixed-mode (RF/digital/analog) circuits, where signal excursion is limited by supply voltage. It provides very good DC simulations, and reasonable RF simulation, over the first quadrant of the I-V plane, for reasonable drain currents at or below Idss. TOM-3 model accurately predict DC operating point in a self-biased circuit application and is SPICE-compatible. TQT has adapted this model to microwave applications of pHEMT devices, but caution must be used due to certain model characteristics and limitations.
In a current-limited circuit configuration, the TOM-3 model tends to over-estimate power performance.

This is the direct result of the model having no inherent Imax (maximum drain current) limit. In other words, increasing gate voltage above that produces Imax (normally associated with zero depletion depth) results in a continued and unrealistic increase in drain current. This inaccuracy becomes apparent at gate voltages above $V_{gs} = 0V$.

5.3.1.3 EEHEMT (WIN Semiconductor, Triquint) [237]

EEHEMT is an industry-standard nonlinear model incorporated in both the ADS and AWR circuit simulators. It may be re-biased over a limited range of voltages and currents near the modeled quiescent point. EEHEMT models are typically fitted to large-signal RF measurements (load-pull) in addition to DC I-V, pulsed I-V, and S-parameters.
Figure 5.4 illustrates the equivalent circuit for EEHEMT model.

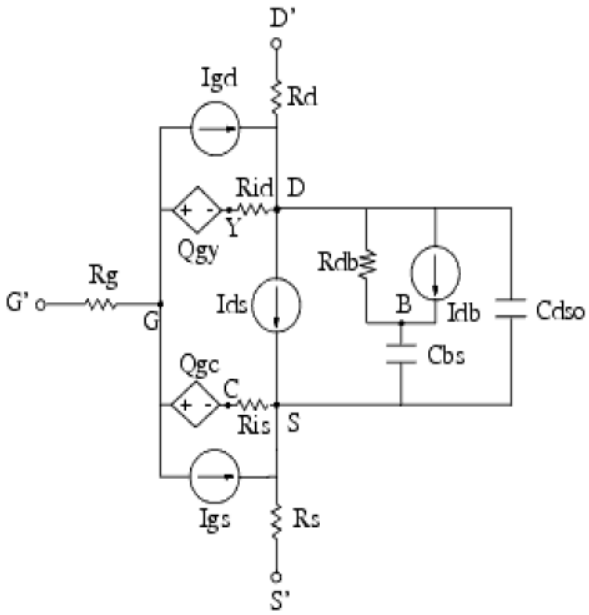


Figure 5.4: EEHEMT equivalent schematic circuit

Agilent EEHEMT model incorporates bias dependence in junction capacitances, an accurate drain-source current model, and accurate prediction of DC and RF Gm-compression characteristics of HEMTs. EEHEMT also incorporates a dispersion model that allows independent and simultaneous fitting of RF and DC characteristics. Nonlinear EEHEMT models are fitted to first-quadrant DC I-V and pulsed I-V, as well as S-parameters at multiple biases, and are verified against single-tone load-pull data at two frequencies. In some cases, the model may be further optimized by comparing simulation results to measured two-tone inter-modulation data. EEHEMT model fitting is more time-consuming than either Materka or TOM-3 modeling. It requires a large data set as well as expert extraction and

fitting, but generally provides improved large-signal simulation at microwave frequencies. EEHEMT model was not developed as Spice compatible. Though the EEHEMT model is inherently re-biasable, this does increase design risk. Suggested limits for re-biasing are +/- 50% change in drain current and +/- 15% change in drain voltage, about the quiescent point for which the model is published. EEHEMT model characteristics are validated against load-pull data at the quiescent bias point only.

5.3.1.4 Agilent HBT (WIN Semiconductor) [238]

Agilent HBT model leverages the essential compound semiconductor physics-based model introduced in the DARPA/UCSD HBT model [239] based on the previous Gummel-Poon BJT model [240]. Significant advances and improvements over this model, as well as a robust implementation in ADS, have been achieved. This makes the Agilent HBT a preferred alternative to Si-based BJT models or university written code for serious and accurate product design in III-V HBT technology.

Figures 5.5 and 5.6 show the large and small signal equivalent circuits for Agilent HBT model.

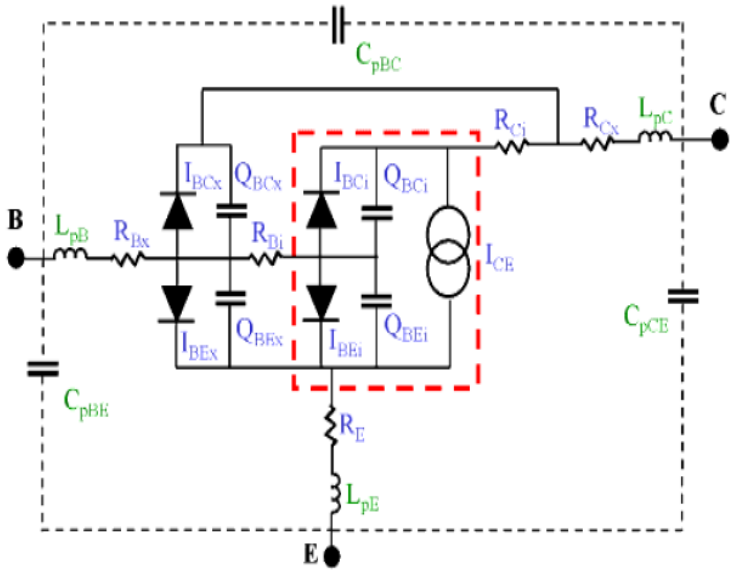


Figure 5.5: Agilent HBT large signal equivalent schematic circuit

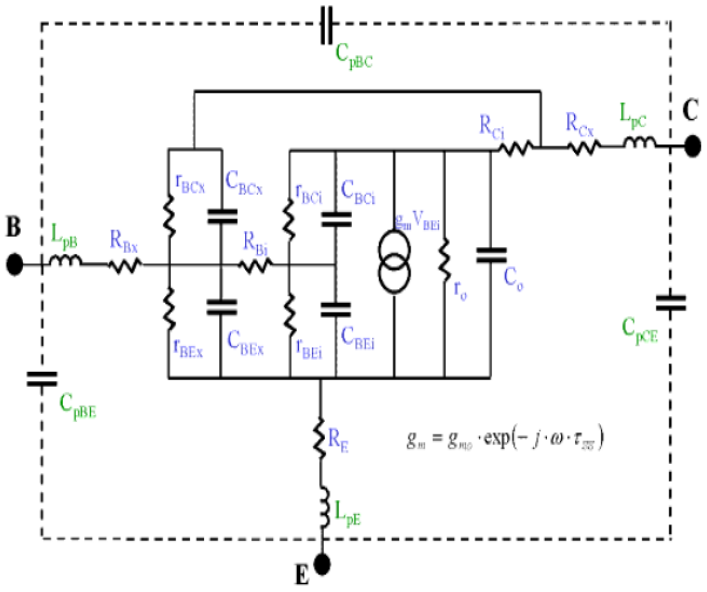


Figure 5.6: Agilent HBT small signal equivalent schematic circuit

The charge model contains a flexible collector transit time formulation that empirically accounts for the electric field dependent electron drift velocity in GaAs and InP collectors. This enables accurate fits of cutoff frequency ft vs. bias over a wide range of bias points, which improves linearity predictions [241].

5.3.1.5 TGMP2 (Triquint HBT) [238]

TGMP2 model provided by Trquint is a modified version of the original Gummel-Poon model [240]. TMGP2 model describes better the junction capacitance, self heating, and size scaling behavior of the HBT, than the original Gummel-Poon model. The TMGP2 model is available in the Agilent and Cadence bipolar design kits.

TMGP2 does not account for breakdown behavior. TMGP2 is scalable for emitter finger number, width and length. The model accounts for temperature and process variations. Non-linear TMGP2 model represents S-parameter behavior with sufficient accuracy for most applications, over a wide range of the output current (Ice)- output voltage (Vce) bias space.

5.3.1.6 VBIC (WIN Semiconductor, IHP) [242]

VBIC includes improved modeling of the Early effect [42] (output conductance), substrate current, quasi-saturation, and behavior over temperature-information necessary for accurate modeling of current state-of-the-art devices. However, with default parameters, the model is equivalent to the Gummel-Poon

model.

Figure 5.7 the equivalent circuit for the VBIC HBT model.

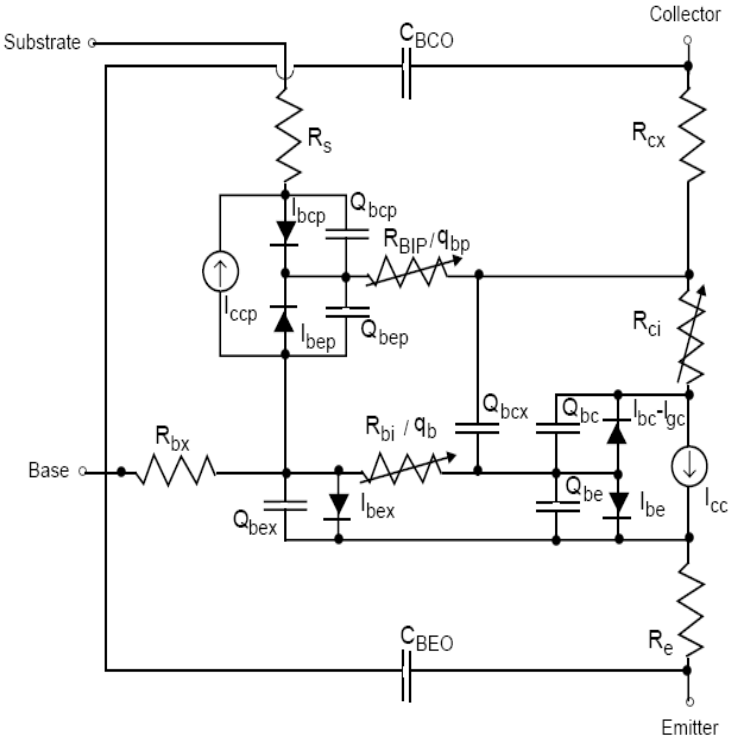


Figure 5.7: VBIC equivalent schematic circuit

Advantages of VBIC over the Gummel-Poon model include:

- An Early effect model based on the junction depletion charges.
- Inclusion of the parasitic substrate transistor.
- An improved single-piece junction capacitance model for all 3 junction capacitances.
- Improved static temperature scaling.
- First-order modeling of distributed base and emitter AC and DC crowding.
- High-order continuity (infinite) in equations.

5.3.2 Compact (Physic) Models Summary

Table 5.1 show a summary of the main features of the physical models for pHEMTs and HEMTs which are a priori the most featured devices to feasibility study.

Model	Materka	TOM-3	EEHEMT
Bias Dependence	no	yes	yes
I-V Symmetry	no	unverified	no
DC I-V Prediction	Yes, Q point	Yes, (id<Idss)	Yes, Near Q point
RF I-V Prediction	Yes, Q point	no	Yes, Near Q point
I-V Data Extraction	Pulsed I-V	DC I-V	DC&Pulsed I-V
RF Data Extraction	S, Q point	S, I-V plane	S, I-V plane (with load pull)
Temperature Dependence	no	no	no
Problematic Applications	RF Linearity, Compression, 3rd quadrant operation, Mixed Analog/Digital	Current Limited load, breakdown behavior, operation above Idss	Transient simulation, high knees voltages

Table 5.1: Compact Models Characteristics

5.3.3 Measurement Based Model (Technology Independent Model)

The internal structure of measurements models is derived from general mathematics, describing externally observable (better known as measured) behavior given an input stimulus and known external conditions. Parameter based for a measurement based model is simply a matter of capturing the associated measurements defining the model in its specified file format. Such 'black models' ideally relieve the *model- maker* from knowing the internal structure of the device under test (DUT). While measurement-based models do not immediately allow for process, voltage, or temperature variability, they can be extracted relatively quickly and hide the intellectual property of DUT, which might otherwise be exposed through a compact model parameter set.

Measurement based models have been and are of actual active interest [243], [244], [245]. For example, most of today simulators have a nonlinear amplifier model that takes parameters such as gain 1 dB compression point (P1dB) and uses a relatively simple nonlinear input-output function (polynomial) to give first order gain compression.

In the following, among the many available behavioral models provided by EDA Tools software companies and semiconductor industry, we describe only those models that can be implemented by the available EDA tool at the semiconductor process pre selected for this feasibility study.
We can mention in advance that, depending on the measurement setup, the behavioral model under consideration can by divided in two main groups: those which model is derived with instruments working with input and output impedance terminations of 50Ω and those which use input and output impedance of arbitrary values.

5.3.3.1 S Model (50Ω)

The most simple behavioral model that can be used for the PA description is a small signal S parameter file [246]. S parameters were developed as a method to analyze and model the linear behavior of RF devices and can be used to predict small signal gain and perform budget analysis, but they do have limitations. They are defined only for small signal linear systems and fail to capture harmonic, distortion or other nonlinear effects. As a result, they serve only as a *s*tarting point for further analysis incorporating more complete information. So, measurement of nonlinear behavior of the PA, requires alternative models. Typically, to characterize the nonlinear transfer between the PA input and output, behavioral models are supplemented with nonlinear mathematical expressions as we show in next sections.
Table 5.2 shows the structure of an S parameter model.

Freq.	S_{21} Mag (dB)	S_{21} $Phase$ (Deg)	S_{12} Mag (dB)	S_{12} $Phase$ (Deg)	S_{11} Mag (dB)	S_{11} $Phase$ (Deg)	S_{22} Mag (dB)	S_{22} $Phase$ (Deg)
Freq(1)	...	...	...	...	...	...	...	...
Freq(2)	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...
Freq(n)	...	...	...	...	...	...	...	...

Table 5.2: S parameter table model structure

S parameters are similar to impedance (Z), admittance (Y) or hybrid (H) parameters. The main advantage of the former is that they instead of use of short and open circuit conditions to characterize the electrical network, matched loads are used. This terminations are much easier to handle and design, and even more, they prevent the device from damage avoiding high voltages or high currents at the output when measurement is realized.
S parameters are obtained measuring incident and reflected voltages at the input and output of the device under test (DUT at a bias condition of interest.
The measurement setup is basically the presented in next section (setup 4).

In the following, S2D, P2D and X parameters models are examples of how S parameters can be modified to include the nonlinear behavior. In case of X parameters, as we show next, the S parameter results in a subset of the X parameter under small signal excitation.

S parameters Remarks:

- S models are 50Ω models.
- S models are obtained with measurement SETUP 4.

- S models requires on wafer calibration kits for error correcting.

5.3.3.2 S2D Model (50Ω)

The S2D model [247] is a measurement based model that captures the small and large signal behavior of a power amplifier (or active device). It is essentially a narrow band amplifier model. It uses measured S parameters for matching networks, and models the large signal amplifier transfer characteristic by fitting a polynomial to the fundamental power out-power in characteristic (Gain Compression). Hence, the polynomial fitting is an odd order polynomial, and only odd order harmonics are produced by this model. The associated S2D datafile comprises a block of S parameter data over a range of frequencies, and a gain compression table (GCOMP), which described the magnitude and phase of gain compression at a single frequency.
Table 5.3 shows the structure of a S2D parameters model.

Freq.	S_{21} Mag (dB)	S_{21} $Phase$ (Deg)	S_{12} Mag (dB)	S_{12} $Phase$ (Deg)	S_{11} Mag (dB)	S_{11} $Phase$ (Deg)	S_{22} Mag (dB)	S_{22} $Phase$ (Deg)
Freq(1)	...	...	...	...	...	...	...	...
Freq(2)	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...
Freq(n)	...	...	...	...	...	...	...	...
P_{in}	S_{21} Mag (dB)	S_{21}	...	...	...	...	...	...
$P_{in}(1)$	...	...	xx	xx	xx	xx	xx	xx
$P_{in}(2)$	...	...	xx	xx	xx	xx	xx	xx
...	...	...	xx	xx	xx	xx	xx	xx
$P_{in}(max)$	...	...	xx	xx	xx	xx	xx	xx

Table 5.3: S2D parameters table model structure

NOTE:In table 5.3 'xx' values means a non required value. The P_{in} values are measured at a single frequency.
The measurement setup is basically the presented in next section. (Setup I + Setup II).The S parameters are obtained as in Setup I, the difference now is that the model includes S_{21} values for pre defined input amplitude values, namely, the AM-AM and AM-PM characterization of the DUT.
In turn, the simulation software shall convert (fitting) the power dependent values of S_{21} to a polynomial description of the DUT to be used with the harmonic balance simulator.

S2D parameters Remarks:

- S2D models are 50Ω models.
- S2D models are obtained with measurement SETUP 4 and 5.2.
- S2D models requires on wafer calibration kits for error correcting.

5.3.3.3 P2D Model (50Ω)

P2D model [247], [248] can be defined as a *p*ower dependent S parameters behavioral model. The P2D format is essentially measurement based, using a vector network analyzer (as previous S and S2D models).
It is a broadband amplifier model based on Large Signal S parameters.
The table model is composed of small signal parameters over frequency and a series of tables of large signal parameters: Each table at a single frequency contains the large signal parameters a as functions of the power incident at ports 1 and 2.
P2D model is monochromatic: works only at a single frequency, it cannot generate the harmonics produced by the nonlinear gain characteristic, but predicts well the gain compression behavior as a function of frequency across the bandwidth of interest.
In terms of limitations, a P2D model, for example, is not the best choice when predicting DUT load pull contours or load dependent behavior.
Tables 5.4 and 5.5 shows the structure of a P2D parameters model.

Freq.	S_{21} Mag (dB)	S_{21} $Phase$ (Deg)	S_{12} Mag (dB)	S_{12} $Phase$ (Deg)	S_{11} Mag (dB)	S_{11} $Phase$ (Deg)	S_{22} Mag (dB)	S_{22} $Phase$ (Deg)
Freq(1)	...	...	...	...	...	...	...	...
Freq(2)	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...
Freq(n)	...	...	...	...	...	...	...	...

Table 5.4: P2D parameters table model structure (linear part)

$P_1(in)$	$P_2(out)$	S_{21} Mag (dB)	S_{21} $Phase$ (Deg)	S_{12} Mag (dB)	S_{12} $Phase$ (Deg)	S_{11} Mag (dB)	S_{11} $Phase$ (Deg)	S_{22} Mag (dB)	S_{22} $Phase$ (Deg)
0dBm	10dBm	...	...	...	...	...	...	...	...
1dBm	12dBm	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...

Table 5.5: P2D parameters table model structure (non linear part)

P2D parameters Remarks:

- P2D models are 50Ω models.
- P2D models are obtained with measurement SETUP 4 and 5.2.
- P2D models requires on wafer calibration kits for error correcting.
- P2D models do not allow inter modulation distortion analysis pr harmonica analysis.

5.3.3.4 S functions Model(50Ω)

S functions are the extension of the polyharmonic distortion modeling approach developed by [246]. They relate the spectra found at a device's terminals for a given set of stimuli and termination impedances. The underground mathematics is the same as for X parameter described in the next section. For the sake of simplicity we not treat this concept here. Interested reader is directed to [249] or [250].
S-functions are able to predict harmonic and modulation behavior of nonlinear devices under different mismatch conditions. As with S-parameters, S-functions can be cascaded to predict nonlinear behavior of circuits and systems.
S-functions are easily determined with the modeling option of the NMDG [251] VNAPlus extension kits. These kits extend various commercially available network analyzers (Agilent and Rohde & Schwarz) using additional hardware and software to characterize nonlinear behavior. The characterization is done in the frequency domain (and can be converted into the time domain) under real life conditions for any terminal impedance by way of load/source-pull.
Microwave Office can import this behavioral model to directly design large circuits using the measured data or to provide more detailed data sheets. On the other hand, neither Agilent ADS or Cadence Virtuoso do accept this behavioral model.

NOTE: Since this table based model run on a software that is not available in the LAPSyC, we discard it as an option for design characterization.

5.3.3.5 X Parameters Model (50Ω)

Other approach for measurement based models starts with the more fundamental mathematics developed under the name of polyharmonic distortion (PHD) models [246]. Here the black box model is represented by a generalized transfer function relating an input signal at any port of observed output signal at all ports. X parameters [249], [252] capture, these transfers functions for both incident and reflected signals under nonlinear drive conditions. By the nature of their formulation, X parameters reduces to S parameters at low drive levels.
The mathematics being applied is an elegant approach to a problem of considerable complexity. In [246], the mathematical convergence of X parameters to S parameters is shown by identifying the X parameter terms arising from harmonic generation and showing how they go to zero under low level drive tone conditions.

Similar to Cardiff model (explained next), there are an elegance and simplicity hiding the complexity. The mathematics at the foundation of X parameters allows interpolation among measured model parameters. Measurement density and discrete parametrization (bias, termination,power level, etc.) causes an explosion in file size as more parameters increase model dimensionality. However, unlike Cardiff model's philosophy (which simulate accurately for only those conditions in which he model has been measured), the philosophy of PHD is to extrapolate from known measured data as well (see for example [253] and [254]).
Today X parameters can be only extracted with Agilent non linear vector network analyzer (PNA X model). There also stand alone modules and software that allows to convert a traditional linear vector network analyzer into a non linear one, for example the company [251]. However, the main drawback of this product is the 'low stable' phase reference for the harmonic phase extraction.

AWR Microwave Office and Agilent ADS can handle in their respective simulators the X parameters behavioral models.

X parameter model Remarks:

- X parameters model is non restricted to 50Ω. The impedances are chose according to needs.
- X parameters model runs in Agilent ADS and AWR Microwave Office.
- X parameter model requires a non linear vector analyzer like PNA X series from Agilent.
- X models are obtained with measurement SETUP 5.4.

5.3.3.6 Cardiff Model

Cardiff Model is a similar (table based) model as X and S parameters, the table relates I-V waveform data at a device's terminals for a given stimuli and set of load/source impedances.
The approach of this measurement based model is to precisely measure what it is potentially simulate, and store the resulting waveforms. A good starting point for such a a measurement based model would be a reasonably small set of parameters. The measurements obtains the incident and reflected time domain current/voltage waveform at the ports of the DUT [255]. The test setup is similar to that of a non linear vector analyzer but uses a sampling oscilloscope rather than a harmonic mixing or sampling in the time domain.
The resulting model uses four table based nonlinear functions representing corrected device currents and voltages to represent device behavior for a given input stimulus, bias,and terminating impedance. The system can employ single or multiple tone large signal measurement, including harmonic load pull.

Once the model is obtained, the Cardiff design methodology allows to observe the voltage and currents waveforms meanwhile harmonic loads are varied in real time. With the harmonic terminations the designer is able to shape the waveform to match the theoretical values that produce optimum results.

The resulting behavioral model, obtained under the load conditions that yielded optimum performance, can be extracted and invoked into the simulation software. As a result, modeling and design engineers can fully characterize their device for any signal level and impedance environment. For the same set of environmental conditions (power drive, bias and terminating impedance), such model should be a more accurate representation of the device behavior compared to a compact model extracted outside of these operating parameters.
Cardiff behavioral model is supported by AWR Microwave Office. Agilent ADS and Cadence Virtuoso do not provide this feature.

NOTE: Since this table based model run on a software that is not available in the LAPSyC, we discard it as an option for design characterization.

Cardiff model Remarks:

- Cardiff model is non restricted to 50Ω. It is mainly extracted at the optimum impedances.
- Cardiff model runs only in AWR Microwave Office.
- Cardiff model requires a high speed sampling oscilloscope for its extraction.

For detailed information on subtle differences between Cardiff model, S functions and X parameters refers to [256] , [257], [258], [259]. Also, for detailed description of how tables are constructed for X parameters and S functions (not described previously for simplicity) refers to [258] and [246]

5.3.3.7 Non 50Ω Behavioral Models

All the behavioral models discussed previously are assumed to be extracted with instruments operating at the standard transmission line impedance, namely, 50Ω. However, it is known that a better model (close the real device) could be obtained if the measurement setup is configured close to the device operating impedance (for example, the AM-AM derived with a 50Ω setup fails to predict the AM-AM behavior for the load changes [260]).
S, S2D and P2D model are in their nature 50Ω models. In opposition, S functions, X parameter and Cardiff models can be extracted with arbitrary impedances.

5.3.4 Models Summary

5.3.4.1 Physical model Summary

Next we summarize the mains aspects of the physical models under consideration:

- Physical models are complex to measure and derive, they are extracted mostly by the foundries or specialized modeling companies.
- Physical device models are critical in the PA design flow. Their selection must be carefully considered.
- When using physical model, the extraction conditions of the model (bias, temperature, impedance, etc) must be take into account.
- Most of the physical models are 'discrete' in the sense that they represents the device physics only at those values were the model was derived.
- For all the semiconductor process under consideration, the available models allows for non linear simulations for PAE and load pull optimization.
- Physical models evaluated do not model the thermal dynamic of the device (critical for PAs design). They offer models extracted at single temperature.

5.3.4.2 Behavioral Models Summary

Next we summarize the mains aspects of the behavioral models under consideration:

- Behavioral models only provides information of the device or circuit for the operating conditions at which the model was extracted.
- S parameters are not enough for the power applications of this feasibility study, providing not many useful information. At least, for design characterizing and further simulation with this data, the use of S2D or P2D models must be considered.
- X parameters are today the most complete non linear behavioral model. The instruments that they requires are expensive.
- Cardiff model, also called 'waveform inspired models', are out of scope since available EDA tools at LAPSyC can not handle it.
- Behavioral models can handle linear and no linear behavior. As the modeling capacity increase it file size increase. There are trade offs to be accounted for.
- Behavioral models are tied to the EDA tool to be used.
- As the behavioral model increase its modeling capacity the cost of measurement instruments to extract it also increase.
- The designed devices or circuits will be delivered together with their respective behavioral models characterized through laboratory measurements.

- Behavioral model can be classified as '50Ω' or non '50Ω' models. The later depends of the instrument impedance used for the model derivation.
- For power application always is recommend to model a device as close as possible to the operating impedance.
- Behavioral model are independent of the used technology allowing intellectual property protection.

5.4 Measurement for Characterization

Following we present an overview of the measurement setup required in this project characterize single devices or circuits with behavioral models (table based models) in order to complete the full design flow (Foundry− >LAPSyC/GISEE− >CONAE). Only measurements for behavioral models are considered since, as mentioned previously, from the perspective of this project compact models are reserved to foundry and specialized companies basically due to the high specialized instruments and human resources required for that purpose (the later falls out the scope of this feasibility project, although should be considered in the future if the general strategy were to get a full control of the technology).

5.4.1 SETUP 1. I-V Measurement

I-V measurement is referred to input-output measurements of current and voltage of a an active device at DC conditions. Is basically related to the characterization of a single device in DC used to setup up the operating class of the device. The measurement can be also applied to multiple devices or even to full circuit design.
I-V measurement requires DC current-voltage controlled sources DC bias tees to isolate the rf signals from DC source and DC current-voltage measurement instruments. See figure 5.21 for a graphic description on how instruments and accessories are connected.

5.4.2 SETUP 2. Thermal I-V Measurement

The previous measurement would not have meaning (for power microwave transistor) if the exact channel temperature at which the I-V values are extracted is not known. Thus, the I-V measurement must be completed with the correct temperature data.
Does exist two different approaches to measure the channel temperature. One is to measure the average temperature of the channel meanwhile the other is to measure the thermal distribution as a function of the physical device dimension. Of course, the second method is the recommended since can prevent from a measure that underestimate the real channel temperature like in the case of an average measure. This approach makes more reliable the measure and consequently the active device design.
Below we present a brief description ob both methods.

5.4.2.1 Temperature measurement

This measure is realized with a thermal infrared camera whose thermal resolution is lower than the physical dimensions for the device under measure. So the measure describe a single temperature value that can not match with the real maximum temperature verified in the channel. We must remember that this maximum (hot spot) is the responsible of the device damage, even most of the device were at lower temperature. This value is commonly verified at the geometric center of the device.

5.4.2.2 Temperature mapping

To avoid the previous mentioned, an infrared camera with resolution close to the transistor's 'fingers' dimension must be used. In chapter 2 was mentioned that for an effective temperature management of high power active devices, they mus the designed with a structure called multi-finger, which means that a single channel high power transistor is replaced by a design of a small channels transistors [261] connected like show figure 5.8.

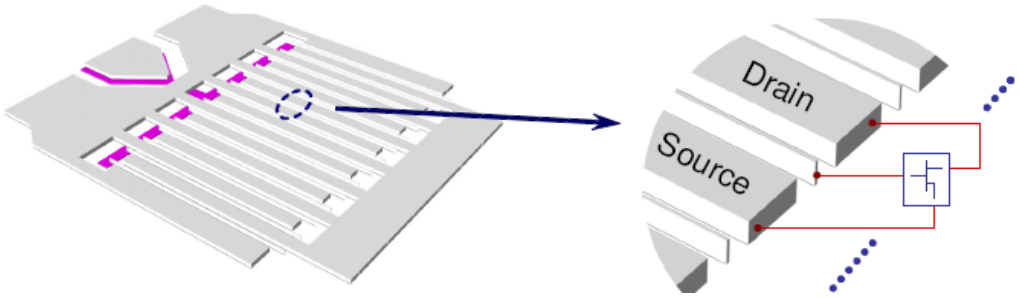


Figure 5.8: Typical Multifigner FET structure for high power devices (From [22])

This design solves the thermal management aspect but suffers from the inconvenient of a non uniform distribution of the temperature across it structure. So, when a design of high power active device is considered, careful attention must be pay to this problem to avoid the origin of hot spot in the multi finger structure that could damage it.
Given that, foundry companies gives not many information about the active device structure (they do not want to reveal their know how) is it mandatory to measure the thermal distribution of the active device in laboratory. This task is usually called thermal mapping.
Figure 5.9 shows a picture of a thermal mapping in a power microwave transistor for a multi finger structure like shown in figure 5.8.

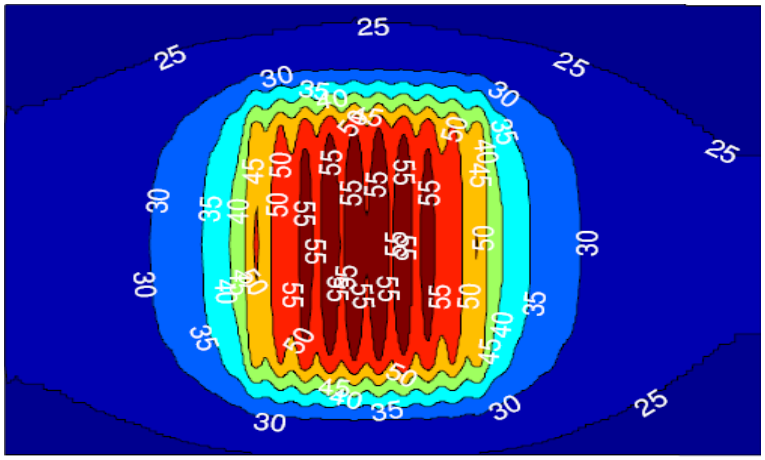


Figure 5.9: (Thermal Mapping of a 10 finger FET cell operating at 0.3W/mm (From [22])

5.4.3 SETUP 3. Pulsed I-V Measurement

Standard DC-IV curves plot drain current as a function of drain voltage for various gate voltages, with a set of drain and gate voltages being continuously applied. A DC bias applied to a transistor may result in device self-heating; the longer the device is on and the more power applied to the device, the more self-heating occurs. By pulsing the bias with sufficiently short pulses and by choosing a sufficiently short duty cycle, the resulting I-V curves will represent the transistor characteristics for quasi isothermal operating conditions. [23]. The duty cycle and duration of the pulse must be calculated to avoid thermal memory and really makes an isothermal measurement. Figure 5.10 illustrates the previous concept.

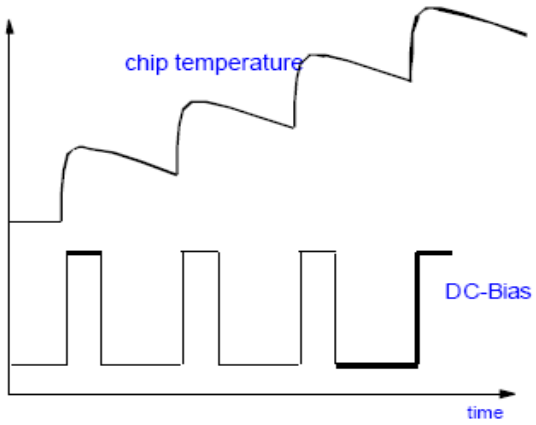


Figure 5.10: Thermal effect of the pulse duration and its duty cycle

Biasing a device under pulsed conditions will change the device S-parameters, therefore it is essential to properly record S-parameters under exact application conditions.
Figure 5.11 shows the difference between the I-V characteristic of a power microwave GaN transistor

with and without consider the thermal effects. Is clearly seen that the model that do not take into account the thermal effect is highly different from real life device, namely, to that which include this effects.

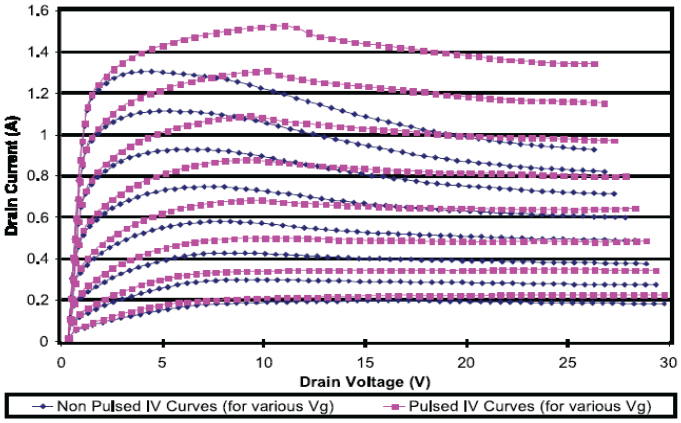


Figure 5.11: Pulsed versus Non Pulsed I-V curves of a GaN transistor

5.4.4 SETUP 4. S Parameters Measurement

Measuring not only the magnitude of S parameters but also their phase offers several benefits such as system error correction, usage of embedding and de embedding, representation in the Smith chart, calculation of the group delay, time domain transformation among others.

The fundamental instrument to realize this measurement the Vector Network Analyzer (VNA). The fundamental blocks of a conventional VNA are shown in figure 5.12. Depending on the measurement direction, the stimulus generator is either routed toward port 1 or 2. The incident wave is tapped to generate a reference channel (by a power splitter). At the test ports, the separation of incident and reflected wave is done by a directional coupler.

Measurement performed include frequency sweep, power sweep and time sweep. Figure 5.12 show a basic of a VNA instrument and how the DUT is connected to it.

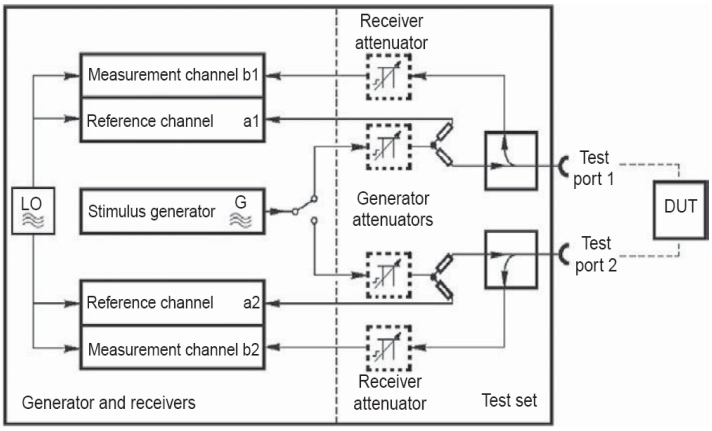


Figure 5.12: Bidirectional two port typical VNA Schematic

5.4.4.1 SETUP 4.1. Hot S Parameters Measurement

The characteristics of PAs is thet they are power level dependent, especially when the amplifiers are operated near their 1 dB compression point. Besides the gain compression of S_{21} other parameter changes their characteristic values, like S_{22}.
The output reflection coefficient, in particular, is of considerable interest since determines the efficiency of the PA and the voltage standing wave ratio (VSWR) at the PA output. Hot S_{22} is a considerably different measurement and its measurement setup is illustrated in Figure 5.13:

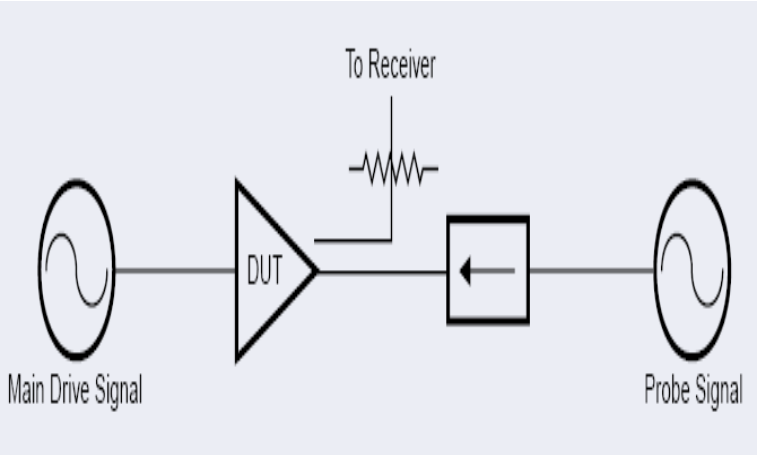


Figure 5.13: Simplified setup for a hot S_{22} measurement

A standard S_{22} measurement would be performed in reverse operation (see previous section). This means that the stimulus at port 1 is switched off, and port 2 becomes the active port. This does not correspond to the original operating condition.

In the hot S_{22} measurement, the amplifier has an input signal at the operating frequency applied to it. The level of this signal is configured such that the amplifier exhibits the output level power that it is designed for. At the same time, a reflection measurement is performed at the output at a frequency slightly different to the input frequency.

Other hot S parameters can be measured also with minor changes in the original S parameter setups. Once the hot parameters are available one, can use it for example, to calculate a new stability factor (K factor) based on them. Now this new K factor is called Hot K stability factor.

5.4.4.2 SETUP 4.2. Pulsed S Parameters Measurements

In many cases, devices need to be characterized using pulsed signals instead of CW signals [23]. Stimulation of the device is provided by either a pulsed RF signal or a pulsed control voltage. One examples of this method are on-wafer measurements of power amplifiers, where heat sinks are difficult or even impossible to implement. Another example is power amplifier modules for pulsed radar systems; such modules have to deliver high peak power and cannot be driven by CW without being destroyed. Figure 5.14 illustrates the thermal effect on S parameters measurement. From this plot it is clear the advantage of pulsed S parameter setups to characterize RF power devices.

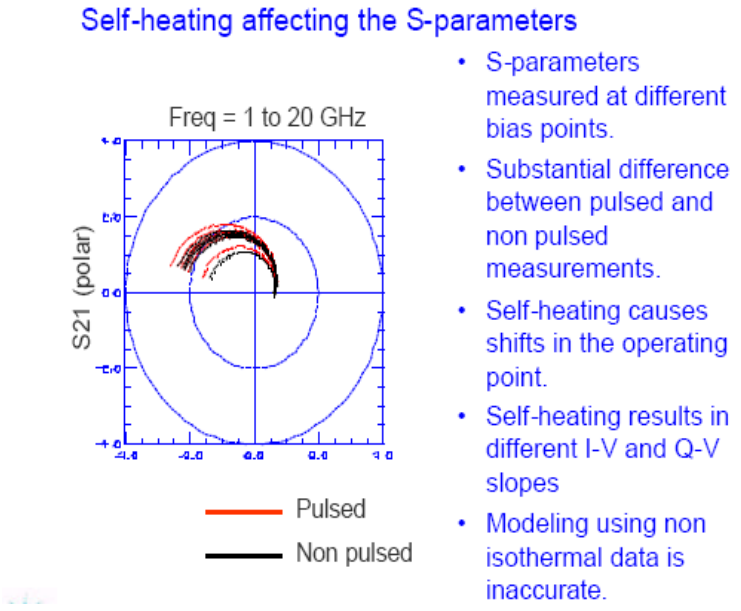


Figure 5.14: Pulsed versus no pulsed S parameter measurement difference (From [23])

5.4.5 SETUP 5. Non Linear Measurements

No linear measurement are intended to characterize the no non linear behavior of the active device which is mostly verified a high power regime. So, no linear measures are principally related to high power measures.
Below we describe the most important measurement setups form the perspective of the feasibility project.

5.4.5.1 SETUP 5.1 AM-AM, and AM-PM Measurement

AM-AM and AM-PM setup measures the amplitude and phase conversion of the transistor (or power amplifier) as a function of the input amplitude. The basic setup is showed below in figure 5.15:

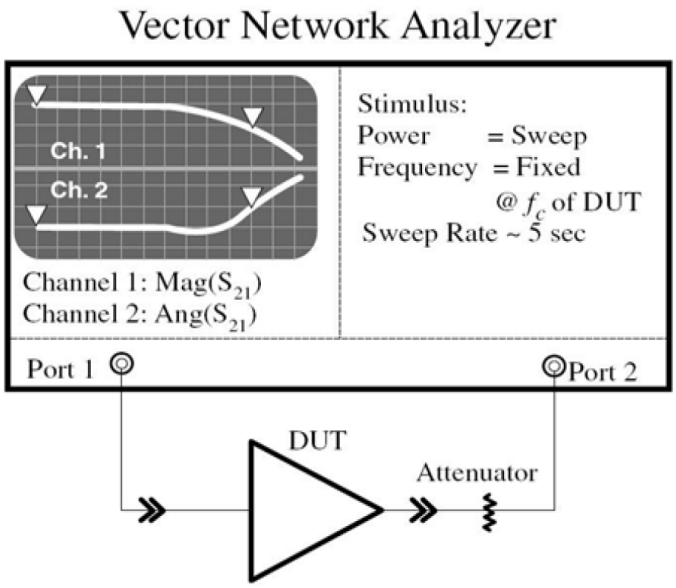


Figure 5.15: Setup for measurement AM-AM and AM-PM characteristic

The main required instrument is a VNA or NVNA (with an extra input power amplifier drive the device to to its no linear regime). Also requires, coaxial adapter and cables and coaxial attenuators..
From the project point of view is not key measure in the current project stage since the first requirements from CONAE were not high linearity amplifiers.

5.4.5.2 SETUP 5.2 1dB. Compression Point, Harmonics Distortion and Interception Points Measurement

This setup is used to characterize the non linear behavior of a power amplifier as a function input signals of sinusoidal type. Is is very useful for amplifiers who amplifies signal with low peak to average

amplitudes distribution. This setup is very important for this project since can characterize very well the nonlinear behavior of the active devices (or amplifiers) close to those conditions for which the designs are intended. Figure 5.16 shows a basic setup to carry out this measures:

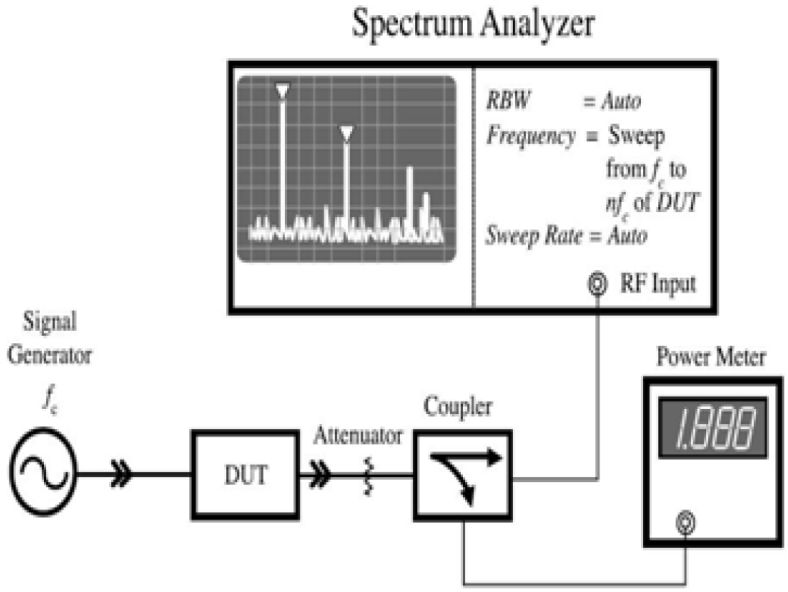


Figure 5.16: Setup for measurement 1dB compression point and harmonics

The main instruments required are: Spectrum analyzer, microwave signal generator, directional coupler, power meter and microwave power sensor (among the coaxial cables, adapters and so on).

5.4.5.3 SETUP 5.3 Inter Modulation Distortion Measurement

It is an improvement of the previous setup 5.2, although as for AM-AM-AM-PM setup, this is intended for high linearity amplifiers measurements. If setup 5.2 can be realized so, this setup results in a redundancy from the project perspective. The basic setup is shown below in figure 5.17:

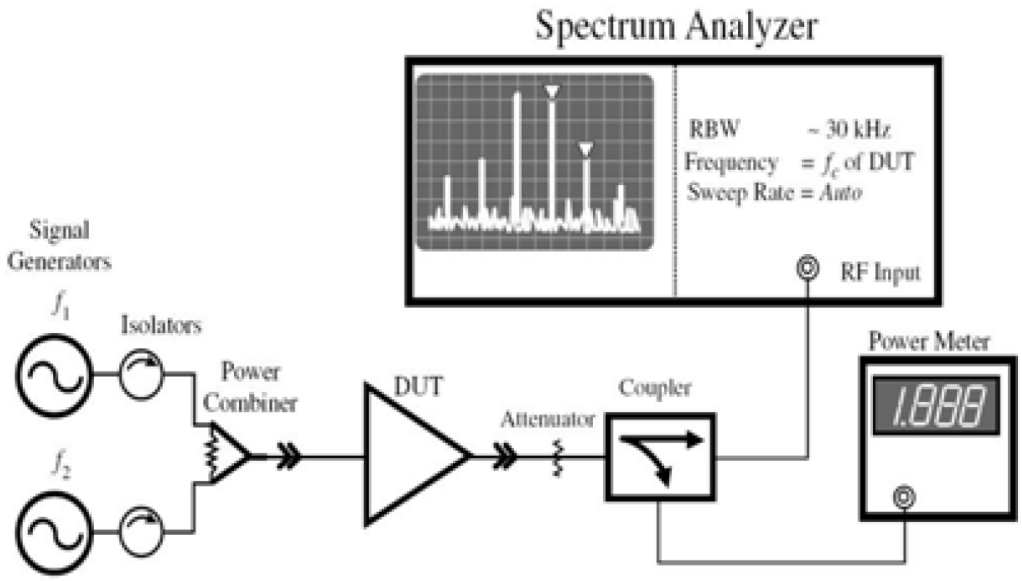


Figure 5.17: Setup for inter modulation distortion measurement

The only extra instrument requirement compared with previous setup is a signal generator that can generate sums of sinusoid signals. Or two separated generators connected by means of couplers and isolators.

5.4.5.4 SETUP 5.4 Non Linear Vector Analyzer

The non linear vector analyzer is able to obtain informations of the amplitude and phase relationships of the device (AM-AM and AM-PM) not only at the operating frequency but also at the harmonics. It represent the most complete and powerful measurement when a high power non linear device design is considered. Huge problems in high power devices like stability can be avoided with the data obtained form this measures. Even more, there are commercial NVNA that allows to convert the measurement directly to non linear behavioral models like X parameters which in turn (used in a EDA tool), derives in a faster and robust design cycle of power microwave devices. The former results more evident when more complex are the designs considered. Figure 5.18 show a schematic configuration of the instrument and how the DUT is connected to it for the measures:

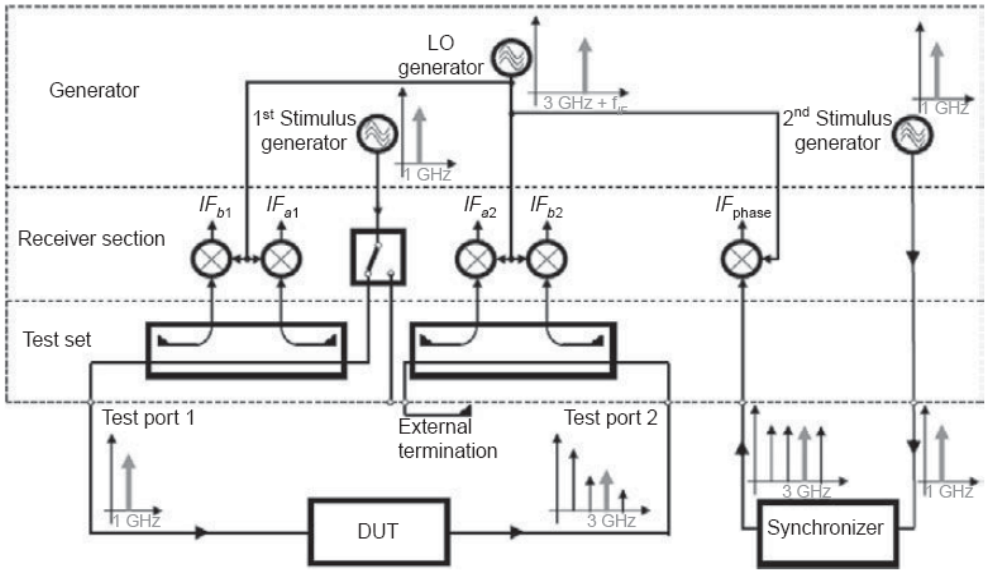


Figure 5.18: Typical Heterodyne NVNA Schematic (A VNA supplement with synchronizer)

The accessories required are similar to those of previous setups except for the frequency operating range. In this setup all components must handle the higher harmonic frequency of interest of this characterization setup.

5.4.6 SETUP 6. Measurements with Source and Load Pull

Load pull consists of varying or 'pulling' the load impedance seen by a device-under-test (DUT) while measuring the performance of the DUT. Source pull is the same as load pull except that the source impedance is changed instead of the load impedance.
Load and source pull is used to measure a DUT in actual operating conditions. This method is important for large signal, nonlinear devices where the operating point may change with power level or tuning. Load or source pull is not usually needed for linear devices, where performance with any load can be predicted from small signal S-parameters.
Figure 5.19 show a basic configuration for source and load pull measurements:

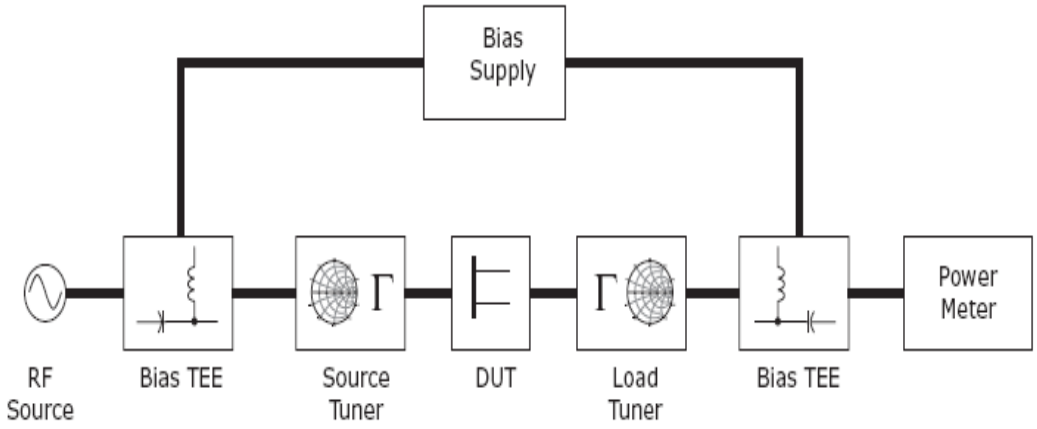


Figure 5.19: A simplified source-load-pull setup

A typical load-pull system consists of the device or amplifier structure under test, electronic or mechanical tuners (whose impedances have been measured previously in many different states), one or more power meters, and associated hardware. As is always the case, output power will be a function of load match. Unlike the small signal case, the relationship will be non-trivial in the large signal limit due to load line limitations along with other issues (even while still quasi-linear). Once the device is operating non-linearly, the relationships become even more complicated. Usually the input tuner is set for something near conjugate match although in highly bilateral devices, the interaction between input and output match can be substantial. The output tuner is usually moved through its various states and the output power mapped as a function of load impedance. A set of constant output power contours on a Smith chart plane of load impedance can then be plotted. This level of characterization is critical for power devices and is usually used to help generate the required matching circuits.

5.4.6.1 SETUP 6.1 Harmonic Source and Load Pull

Figure 5.20 show a basic configuration for harmonic source and load pull measurements.

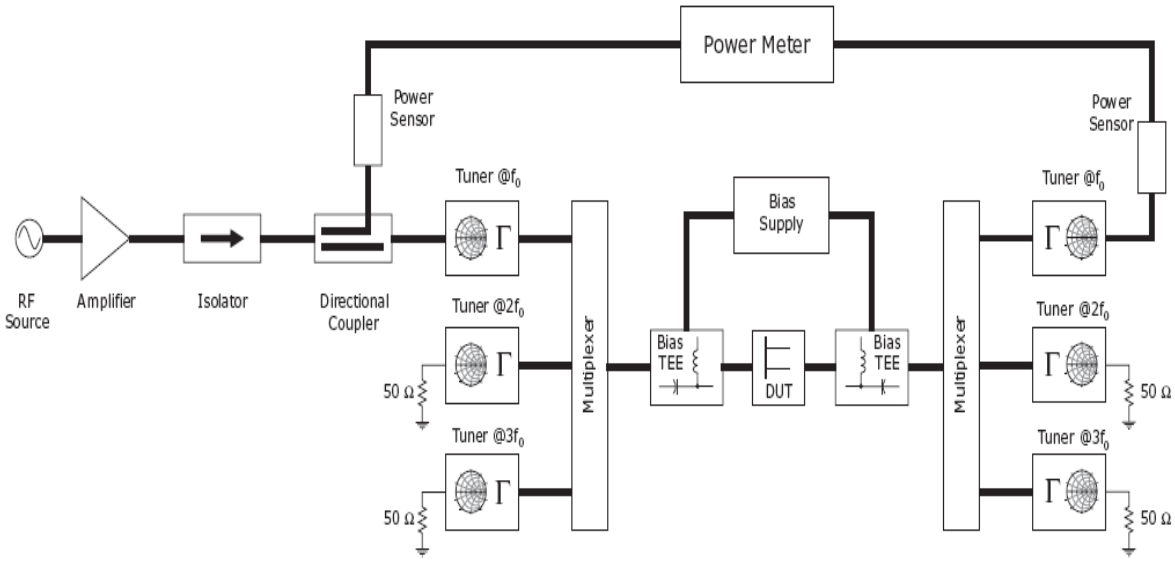


Figure 5.20: An Harmonic source-load-pull setup

5.4.7 Measurements for Characterization Summary

- In this section was presented a review of the measurement setups required to accomplish the project objective.
- There are two main objectives behind the measurements: the first one is to acquire the major possible know how in the design aspects, despite the restrictions (or in some cases lack of information) of the foundry models. The second objective is to characterize the resulted design and construct a good table based model useful in the full design cycle.
- Thermal measurement with high resolution is mandatory. Physics foundry models lacks from complete thermal information or in some case is not available.
- Load pull instruments are mandatory in the project,s context. If high power is required this setup can no be avoided.
- X parameter measurement are highly recommended.

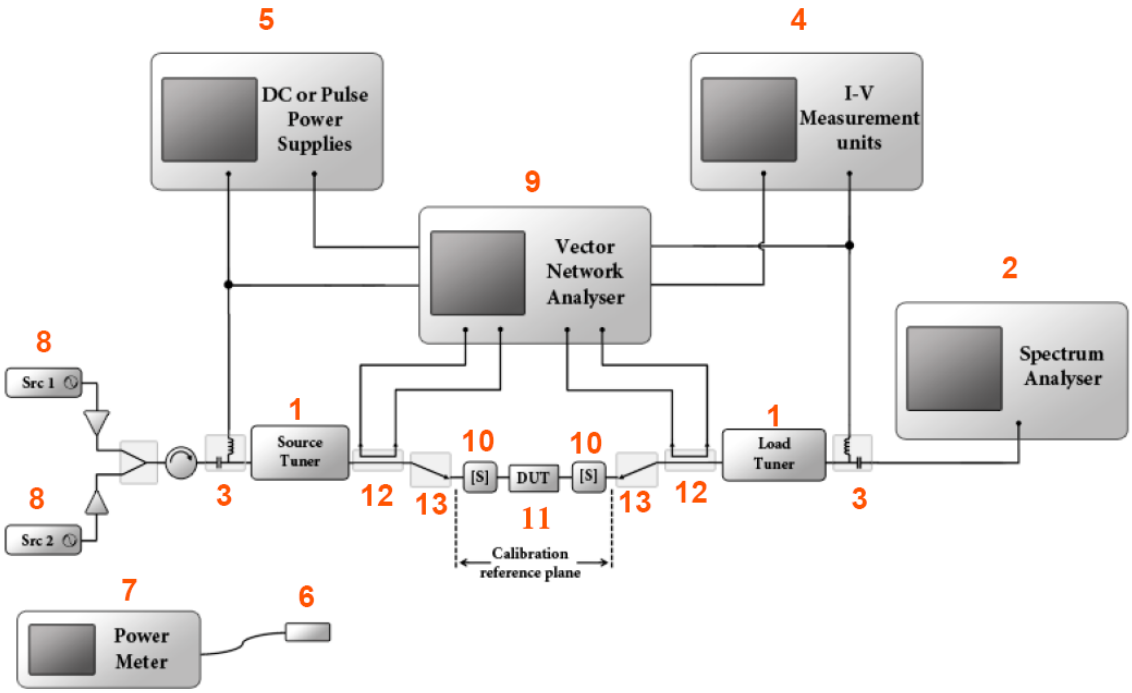


Figure 5.21: General setup for device characterization. Thermal camera is not showed

1. Source and Load tuner for load pull optimization and reliability test.
2. Spectrum analyzer.
3. DC Bias tee or pulsed controlled DC bias tee.
4. DC or pulsed I-V measurement units.
5. DC or pulse controlled power supplies.
6. Microwave power sensor.
7. Microwave power meter unit.
8. Single microwave signal source (can be replaced by a single signal generator with two tone or multi tone capabilities).
9. Linear or non linear vector analyzer.
10. Calibration kits for error de-embedding.
11. Device under test (on wafer).
12. Directional or bi-directional couplers.
13. Coaxial adapters.

Chapter 6

Radiation and Reliability Tests Analysis (Third Deliverable Document)

This Chapter presents basic concepts related to radiation effects and reliability aspects focused on semiconductors used for microwave power applications.

First, a brief description of the radiation characteristics of GaAs and GaN semiconductor devices is described. Also, a review of the current state of art of the research in this subject is described.

Second, basic reliability concepts are presented providing a necessary background to understanding the reliability for specific devices, their failure mechanisms and the available reliability test.

Individual summaries for both, radiation and reliability aspects, are presented to highlight those issues of concern for this feasibility project.

6.1 Radiation Effects in RF Devices

GaAs have been the traditional material since years 90's for RF space applications systems, for that reason, there is a large number of studies on the effects of space radiation on GaAs based devices such us solar cells or GaAs-based light-emitting diodes, although, GaAs-based RF devices have not been the subject of as many studies. One of the reasons is that it is very difficult to degrade GaAs-based RF devices with radiation; they are viewed as 'radiation hard', and are considered robust for many space applications.
From a device point of view, we have three radiation-induced phenomena:

- *Effects from total ionizing dose (TID).* These originate from ionizing radiation damage induced by incident charged particles: protons, electrons, or photons.
- *Displacement damage (DD) effects.* There can be displacement damage on the semiconductor crystal lattice related to incident particle interactions with the semiconductor lattice atoms.
- *Single-event effects (SEE).* These are associated with very high energy particles, protons, and neutrons of high atomic mass cosmic rays. This type of ionization damage in devices has involved the isolating oxides, also the oxide to semiconductor interfaces. It is thus usually relevant to device surfaces and interfaces. Cosmic ray induced SEE are often associated with data loss or error generating phenomena in switching circuits, and they are considered 'soft errors'. Even GaAs devices suffer from poor single-event upset (SEU) immunity at high data rates. Tolerance or hardness to SEU sometimes requires new design architectures, so 'radiation hardening by design' can be achieved.
  Protons are considered the worse case for radiation effects since they produce both ionizing and displacement damage. Radiation from energetic protons in space usually comes from three main sources: (i) the Van Allen radiation belts, (ii) solar proton events/solar energetic particles, and (iii) galactic cosmic rays. Van Allen radiation belts have many protons in the energy range of 1-10 MeV. There are higher energy protons out there, but at much smaller fluences. Most of the protons that electronic devices are likely to encounter in space are in the 1-10 MeV range.

6.1.1 Radiation Testing

Testing for radiation effects is traditionally done at around 100 MeV, 50 MeV, 10 MeV, and 1-2 MeV. The energy used in most of the radiation reports on RF devices (mostly on different types of HBTs) is 46 MeV. This indicates an important gap in the data, and more need for radiation testing with protons in the range 1-10 MeV. Since high energy protons are less damaging because they deposit less energy in the active region of the device, testing only with protons around 50 MeV could give deceptively optimistic results. More testing should be carried out at the lower proton energies, which are known to be more damaging to the active areas of HBTs and other GaAs devices.

6.1.2 Radiation Effect in RF Compound Semiconductor

A study comparing the effects of gamma irradiation on SiGe and GaAs HBT technologies [262] showed that both SiGe and GaAs HBT technologies are tolerant to gamma radiation up to 1 Mrad(Si). Gamma radiation does not cause displacement damage though. The authors in the aforementioned study measured effects on DC and RF performance as well as their low frequency noise, and they did observe more degradation in low frequency noise from the GaAs HBT devices. There has been significantly more research on radiation effects on SiGe HBTs, which encompasses effects of electron, proton, neutron, and gamma irradiation on these devices. The fewer studies done on the III-V devices show good promise for radiation hardness in GaAs and InP-based HBTs, and even greater hardness for the GaN-based devices. Some of the additional work that has been done on these RF materials systems includes the effects of proton irradiation on AlGaAs/GaAs HBTs [263], GaN HEMTs [264], and AlGaN/GaN HEMTs [265]; and the effects of neutron, proton, and electron irradiation on InGaP/GaAs HBTs [266].

6.1.3 Radiation Summary

Some remarks related to radiation effect in RF compound semiconductors are given below:

- The study of radiation effects on power RF devices is quite new, however already have been published works that shows the inherent high radiation resistance of GaAs and GaN devices if compared with CMOS.
- The radiation tests required are similar to those applied to CMOS semiconductor.
- The radiation effects appears of secondary concern in the project's context. However, prior to the final design, radiation hardening techniques should be evaluated carefully.

6.2 Reliability or RF Semiconductor

A definition of reliability is a performance attribute that is concerned with the probability of success or frequency of failure and can be defined as:

- *The probability that an item will perform its intended function under stated conditions, for either a specified interval or over its useful life.*

Another different definition for reliability is:

- *The ability of a product to function under given conditions and for a specified period of item suffering performance degradation beyond a defined limit.*

Generally, reliability is treated as a statistical problem, being a mathematical relationship to approximate the actual failure distribution that takes place when devices are subjected to stress and/or operated for a extended time.
Reliability testing is usually done with a relatively small test sample, using the results of the sample test to make a statistical estimate of the overall reliability and failure rate of the parent population.

6.2.1 Reliability Goals

Reliability goals are determined with respect to each of the four components expected within the definition of reliability. The elements of reliability goals are shown below with examples:

- Performance component: operation within specified data sheet parameters;
- Conditional Component: at an operating transistor temperature of 150 C;
- Failure criteria: minimize or eliminate early failures. Keep the overall failure rates below 0.001%/1000 device hours:
- Time component: extend the useful life of MMICs greater than 20 years (175.000hour);

for the above mentioned a well described reliability goal example might be:

- *Power amplifiers are expected to operate within all data sheet parameters at an operating transistor temperature up to 150 C with less than a 0.001%/1000 failure rate for a 20 year lifetime.*

6.2.2 Semiconductor Reliability Strategy

The strategy to accomplish and verify the reliability goals involves accelerated testing of the circuit and individual building blocks [267]. These building blocks are labeled 'elements', and they consist of each metalization interconnect type, resistors, capacitors, contacts, and active elements of transistors and diodes. 'Element' testing is optimal for a number of different reasons. It is essential to isolate and asses all the various failure mechanisms possible for an amplifier. 'Element' testing is especially useful to the circuit designer because the data can be used to model the reliability performance of circuits based upon physical sizes and operating conditions of each portion of the design. 'Element' tests are used to verify, and in some cases, modify design layout rules.
The mentioned above implies that is it necessary and beneficial to include multiple design copies of single 'elements' for reliability test in the 'Test Characterization Vehicle (TCV) Chips' to evaluate their reliability. The number of copies will depend on the available budget.
The TCV Chips are mandatory to characterize a new technology, thus if we could add extra elements

for reliability tests it would result in a more complete test of such technology.

The reliability strategy involves the following steps:

1. Conduct fundamental reliability studies to identify and measure wear-out mechanisms for each amplifier process.
2. Calculate failure rates of each amplifier element. Continue process improvements until each element's exceeds the goals.
3. Model how temperature, voltage, current density, and other operation conditions or environments affect the time to failure of each element.
4. Select the maximum rating for each element, consistent with the reliability goals.
5. Verify compliance to reliability expectations with reliability qualification testing of the completed amplifier product.
6. Establish the maximum ratings and conditions with the amplifier description (data sheet)
7. Monitor amplifier reliability and compare results with reliability expectations based on element predictions.
8. Re evaluate elements as necessary and life test circuits as improvements or changes are made to processes or designs.

6.2.3 Failure Mechanisms

Failure mechanisms can generally be differentiated intro three types of physical structure: metalization, dielectric, and semiconductor. Here we will not describe a detailed explanation of failure mechanisms since the aim is to present an overview to analyze what type of reliability tests and methodologies could be required to achieve the scope of a future design project (to deep understanding on the subject refers to [268]).
Continuing with the mentioned previously, our interest is on reliability for compound semiconductors since they are the appropriate devices for power microwave transistors and MMIC design. For that reason, below we presents a brief description of most common failure mechanism of compound semiconductors.

6.2.4 Reliability in RF Compound Semiconductor

In compound semiconductors, crystalline defects are far more important than for silicon semiconductors [269] . Failure modes for some compound are heavily influenced by crack or dislocations, which are

of second order of importance in silicon.
Consequently the approaches to reliability that have been demonstrated for silicon are not always applicable to compound.
Another point to keep in mind is that manufacturing technology tends to evolve in ways that suppress key reliability problems. Thus, technical issues that are widely studied during the years that new device structures and materials are developed often become irrelevant once the technology enters in production.
For compound semiconductors the failure mechanism are mainly based on the following mechanism (ee for details [269]):

- *Gate Sinking*
- *Contact Degradation*
- *Hydrogen Poisoning*
- *Hot Carrier Degradation*
- *Passivation Layer Traps*
- *Gate lag effect*

6.2.5 Reliability Test Methodologies

The traditional methods for reliability test are based on mechanisms for failure acceleration. Nearly all reliability work is based on these methods, where a small population of device operate under elevated stress over a relatively short time interval. The failure rate of the sample used for accelerated test can be applied to devices that operate under normal conditions, based on assumed temperature dependence for the failure rate (as well as other acceleration factors)
There are three failure acceleration methods [268]:

- *Thermal Acceleration:* The majority of reliability mechanism are strongly temperature dependent [270]. The failure rate usually increases with temperature. The temperature dependence of thermally activated processes can be often described by the Arrhenius equation:

$$R = A.e^{-E_a/kT} \tag{6.1}$$

  where R is the failure rate, A is a constant of proportionality, E_a is the activation energy, which is constant for a specific failure mechanism, T is the temperature and k is the Boltzman constant.
  The temperature dependence of a particular failure mechanism can be determined form the Arrhenius equation, yielding the relationship:

$$ln\frac{t_2}{t_1} = \frac{E_a}{k}\left[\frac{1}{T_1} - \frac{1}{T_2}\right] \tag{6.2}$$

where t_1 and t_2 are the measured time to failer based on experimental results for two different sample populations that are stressed at temperatures T_1 and T_2.

- *Current Acceleration:* Relationships have been developed to describe the failure rates for metalization or contacts failures as a function of power. However, some mechanisms become important only when the internal current density exceeds threshold conditions [271].
- *Voltage Acceleration:* The electric field is important for mechanisms that depend on hot carriers, impact ionization and specific mechanism for III-V devices such as a current collapse. An acceleration factor must be developed for the electric field, which depends on the specific mechanism and technology. An exponential dependence as next equation is usually used:

$$A = e^{\left(\frac{E_2 - E_1}{\beta}\right)} \tag{6.3}$$

6.2.6 Reliability Summary

- Reliability tests are based on acceleration mechanism (thermal, voltage or current). To carry out these tests are necessary specifics instruments, like an infrared camera or two input-output load-tuners. Thermal acceleration is the most used method.
- To make reliability tests is required to design a number of devices copies of the 'element' under test to acquire the better possible statistical information.
- Compound semiconductor has its own failure mechanism that must be taken into account prior to a reliability test setup configuration.
- We need to keep in mind that although sample testing and statistical model are widely used, conclusions based on sample testing (TCVs) ultimately depends on how well the actual failure distribution of the parent populations obeys the function that is assumed for the overall failure distribution, as well as assumptions about the acceleration factors.
- The estimation of a necessary or minimum number of 'element' samples should be included in the TCVs designs if project's budget allow it.

Chapter 7

Feasibility Study General Conclusions (Fourth Deliverable Document).

In this Chapter we present the final conclusions of this feasibility study. They are based on the material presented and analyzed from Chapter 1 to chapter 6. Chapters 8 to 10 presents an additional material in order to self contain the widespread subject treated in this work, however, their lecture is not necessary to understand the results presented here and is leaved to the interested reader.

The Chapter is organized as follow: First we describe the criteria used to select each foundry and each semiconductor process. These is accompanied by a ranking of the processes constructed according to the mentioned criteria. Second we present what could be expected from each process in terms of power and frequency in function of the current and possible future requirements. Finally, we enumerate the final conclusions of what is feasible with the available resources at LAPSyC and what resources needs to be acquired to achieve the CONAE's design specifications.
After that we mention that, to complete the current study, a working plan of three years for design power microwave transistors and MMICs shall be delivered together this document (it is delivered by separated since falls outside the scope of this study). This plan will include a detailed description of all the required resources described in the conclusions section and a schedule of the tasks required to accomplish the design objectives.

7.1 Foundry's Processes Evaluation & Selection

For the selection of a foundry company and a semiconductor process we used two criteria: the first one can be named the 'commercial' criterion and the second one the 'technical' criterion.
For the 'commercial' aspect we evaluate: pricing, wafer availability and shared wafer configurations, measurement services, dicing, training availability and technical support. Also we include in the evaluation a qualification of the support offered by the foundries during the process of process design kits (PDKs) acquisition and installation and also in the quotation stages which required highly specialized technical support.
For the 'technical' aspect we evaluate the process using the respective PDKs in the EDA tools (ADS and Cadence). We evaluate single design at each process in order to validate, vknee voltage (efficiency), breakdown voltage (reliability), maximum drain current (output power), frequency behavior (gain), non linear model complexity and extraction techniques, among other aspects.
Next, we present a ranking which is a result of a weighted evaluation that contemplates all of the above mentioned aspects ('commercial' and 'technical').
The ranking is presented next in a separated way for GaAs and GaN processes since it is more simple to evaluate.
After that, we present the four process pre selected preliminary to be evaluated with laboratory measurements.

7.1.1 Foundry Ranking

A preliminary ranking of the semiconductor processes (either GaAs or GaN) is presented next. This ranking could change in future during the design stage since, the true specifications and process behavior, only can be evaluated measuring the designed circuits in the laboratory. Further evaluation of the foundry services, both, commercial and technical, will be carried out and also can result in a new ranking classification. Of course, this ranking shall be used to decide on the final process selection which will be only one among the four processes pre selected is this study.

7.1.1.1 GaAs Ranking

The GaAs processes ranking is shown below in Table 7.1:

Process	0.25 XKu	PPH25X	PP25-21
Foundry	Triquint	UMS	WIN Semi
Rate	1st	2nd	3rd

Table 7.1: GaAs processes ranking

Tale 7.2 shows a detailed description of the GaAs process characteristics, not all the evaluated characteristics are shown for simplicity:

Process	0.25 XKu	PPH25X	PP25-21
Foundry	Triquint	UMS	WIN Semi
Ft (GHz)	60	45	60
Size(μ m)	0.25	0.25	0.25
Shared Runs	6	2	12(full wafer)
Power Gain(dB)	17	not available	15
Power Density(W/mm)	0.67	0.90	0.98
Operating Voltage(V)	9	9	10
Training	yes	yes	no
Handbooks	very goog	poor	very good
Models	best	good	very good
Scalable Cells	yes	yes	yes
Commercial Products	TGF2021-12	CHA715-99F	no

Table 7.2: Characteristics evaluated for the GaAs processes ranking

7.1.1.2 GaAs processes remarks

- GaAs process selected covers the 95% of the GaAs foundry market.
- All of GaAs process has its scaled commercial products, namely, process at 0.15 μm.

7.1.1.3 GaN Ranking

The GaN processes ranking is shown below in Table 7.3:

Process	0.25 GaN	GaN 2C	0.25 GaN	GaN 1C
Foundry	Cree	RFMD	Triquint	RFMD
Rate	1st	2nd	3rd	4th

Table 7.3: GaN processes ranking

Tale 7.4 shows a detailed description of the GaN process characteristics, not all the evaluated characteristics are shown for simplicity:

Process	0.25 GaN Cree	0.25 Triquint	0.50 GaN1 RFMD	0.50 GaN2 RFMD
Ft(GHz)	18	32	11	9
Size(μm)	0.25	0.25	0.50	0.50
Shared Runs	4	6	12	12
Power Gain(dB)	9	10	8	6
Power Density(W/mm)	4	6	7.5	4
Operating Voltage(V)	28	40	48	48
Training	no	yes	no	no
Handbooks	no	good	good	good
Models	good	best	good	good
Scalable Cells	yes	yes	yes	yes
Commercial Products	CMPA801B025	TGF2023-20	RF3930D	RF3930D

Table 7.4: GaN processes ranking

7.1.1.4 GaN processes remarks

- UMS GaN process: UMS GaN process is announced to be launched before 2012 Spring season (Europe). Depending on the project launch date and the process specs delivered by the manufacturer this process shall be evaluated and compared to the pre selected process at the end of this report.

- WIN GaN process: WIN GaN process is announced to be launched at the beginning of year 2013. Depending on the project launch date and the process specs delivered by the manufacturer (they claim to equate Triquint process) this process shall be evaluated and compared to the pre selected process at the ending of this report. One of the interesting aspect of this foundry is that they do not present any ITAR restriction.

- Triquint GaN processes: This process represent the state of art among all offered GaN processes. To the end of this report we could not get the PDKs since the process is in a preliminary commercial launch phase. According to the project launch date we must ask again for the commercial status at this moment. It is highly recommended work with this process.

7.1.2 Process Pre Selection

We pre select four process for laboratory evaluation prior to the final selection. We propose this intermediate step since all process offers quite similar specifications and foundry services. In turn, a future evaluation phase must be carried out measuring the performance at the laboratory in order to evaluate and select the definitive semiconductor process.
Among the four pre selected process there are three GaAs process and one GaN process.

We consider that the main strategy is decide for one process among the four pre selected process, although, we consider that would be a reasonable and beneficial strategy to decide for two processes at same time, one GaAs and one GaN, instead of only one of them. The reasons behind this recommendation rely on the limitations that each technology inherently has, namely, the frequency for GaN and the power for GaAs. Thus, handling both technologies and thinking in future CONAE's applications there will be no restriction to growth either in frequency or power, using the best profiled technology according to the requirements.

The semiconductor process pre selection are shown below in Table 7.5:

Process	0.25 GaN	0.25 XKu	PPH25X	PP25-21
Foundry	Cree Inc.	Triquint	UMS	WIN
Device	HEMT	pHEMT	pHEMT	pHEMT

Table 7.5: Semiconductor Process Pre Selection

The pre selected process could change at time the design project were started. The semiconductor industry shows itself a very dynamic behavior in its products so, this pre selection is valid only to date of this report were presented and this pre selection must be revisited if the project funding is delayed a more than three months.

7.2 Selected Processes resulted the State of Art Processes. What we could design with them?

Both selected semiconductors processes, GaN and GaAs, can accomplish with the CONAE's design requirements. The main differences one each other arise in their future expandability in terms of frequency and power. GaN processes are bounded in frequency, they can hardly reach frequencies above 12GHz. By the other side GaAs processes are bounded in power, they can hardly reach power above 10W or better said, to achieve high powers the complexity of the circuits increase rapidly.

7.2.1 With GaAs processes

With GaAs processes can be designed (up to 12.4GHz) power amplifiers up to 15Watt with an important number of active devices, i.e. 8 to 16.
Integrated designs can be easily expanded to frequencies of 35GHz with power in the range of 10Watts (continuous).

7.2.2 With GaN processes

With GaN processes can be designed (12.4GHz maximum) power amplifiers up to 25Watt with a few number of active devices, i.e. 4 to 8.
Integrated designs can be easily expanded to output powers of 50W continuous wave or 250W in pulsed operation.

7.3 General Conclusions

Considering the aspects presented and studied in current and previous Chapters of this feasibility study we conclude that: **IT IS FEASIBLE to design in our Laboratory microwave power transistors and MMICs in L, S, C and X bands with GaAs and GaN semiconductors**. That is, we could deliver designs from frequencies ranging around 0.8GHz up to frequencies in the upper limit of X band, 12.4GHz. The devices can be manufactured to reach continuous output power exceeding the 10 Watts in the X band. The maximum achievable output power could be higher than 10Watts if the frequency requirements decrease.

The final semiconductor material shall be selected among two: Gallium Arsenide (GaAs) or Gallium Nitride (GaN).
The active devices that must be used are two: High Electron Mobility Transistor (HEMT) or pseudo-morphic High Electron Mobility Transistor (pHEMT).

Following, the above results must be completed with a general evaluation of what resources are available and what resources are not available at LAPSyC/GISEE in order to carry out a future project in the near term.

So we present next, a brief description of the available resources and an evaluation of the required resources at LAPSyC/GISEE:

Available Resources: Current resources available at LAPSyC/GISEE needed to design microwave power transistors and MMICs.

- *Semiconductor Processes and Foundry Services:* Four semiconductor processes are available today at LAPSyC/GISEE, they are: 0.25 microns HEMT GaN from Cree Inc., 0.25 microns pHEMT GaAs from UMS, 0.25 microns pHEMT GaAs from Triquint Semiconductor and 0.25 microns pHEMT GaAs from WIN Semiconductor.
  The four process have their process design kits installed, tested and verified in the laboratory

computers and in the EDA server machine (in Cadence and ADS softwares).
The four process have their NDAs documents signed according to each foundry legal requirements.

- *Human Resources:* The current human resources at LAPSyC/GISEE can handle a future project intended to design the evaluated devices and deliver the required results in a reasonable time constraint.
- *Laboratory Instruments:* The current configuration of the LAPSyC/GISEE allows measurements of S parameters up to 24GHz, either at wafer level or DUT level.
- *EDA Tools:* The LAPSyC/GISEE count with both state of art EDA tools, Cadence and Agilent ADS. Both tools are licensed with academic permission. Both software runs either on stand alone personal computers or on a IBM server. ADS software is installed on Linux system and Windows system.

Required Resources: Resources not available at LAPSyC/GISEE to date that are needed to design microwave power transistors and MMICs.

- *Semiconductor Processes and Foundry Services:* Not required. Resources acquired during the feasibility study stage.
- *Human Resources:* The human resources must be trained at foundry companies as soon as possible once the project is started in order to narrow the foundry related problems. Assistance to microwave congresses and internship or cooperation with specific academic institution are highly recommended.
- *Laboratory Instruments:* Basically the instruments that must be acquired are those intended for:

  1. Thermal mapping and measurement at chip size scale (few microns) either at wafer level or at DUT level (Setup 2, chapter 5).
  2. Pulsed I-V measurement either at wafer level or DUT level (Setup 3, chapter 5).
  3. Pulsed S parameters measurement either at wafer level or DUT level (Setup 4.2, chapter 5).
  4. Power harmonics measurements either at wafer level or DUT level(Setup 5.2, chapter 5).
  5. Nonlinear characterization for model extraction and evaluation either at wafer level or DUT level (Setup 5.4, chapter 5).
  6. Input output impedance measurement at high power regime either at wafer level or DUT level (Setup 6, chapter 5).

  Due to the complexity of the above requirements a separated document including the details of the different setups, prices, quoting and configuration combinations will be presented together the this document.

- *EDA Tools:* Not required. Resources acquired and full filled during the feasibility study stage.

Finally, to complete the above mentioned, we want to remark the following aspects.
First, according to the feasibility study results and considering the CONAE's requirements, the design of a single power transistor or a MMICs intended for microwave amplification resulted in a design that implies to handle the state of art in many technological aspects such as: design techniques, EDA tools, semiconductor technology, packaging an so on. Thus, one of the main conclusions of this feasibility study is that to complies with CONAE's requirement the LAPSyC/GISEE have to reach the state of art in the area of microwave integrated circuit with all their implications.
Second, continuing with the above mentioned we present (in a separate document) a working plan of 36 months to reach the technological state of art in this area. This plan contemplates the requirements for human resources and laboratory instrumentation. Also is presented a schedule with the steps to gain insight of the key technological aspect of each microwave semiconductor technology.

As can be seen from the previously mentioned, the pursued goal are quite ambitious if contrasted with the starting point, however, the present report and the attached working plan shows clearly that it is feasible to carry out the scope of the project with a high degree of success probability. Even more, we consider that during the current feasibility stage we already done approximately a 10-15% of the total work required to complete the project scope.

Chapter 8

Thermal Aspects

This chapter presents a basic theory formulation for thermal design of power transistors, including equations, figures and references. The main intention is develop a minimum self contained material of the subject under study that serves of guidance during the feasibility study and also be useful for discussion template between involved organisms (IIIE -CONAE).
The material presented in this Chapter is thought to support concepts related to the *D*esign Strategy presented in Chapter 2 (First Deliverable Document).

8.1 Introduction

The thermal design of a power amplifier is an important part of the overall amplifier design. Is well known that a difference in junction temperature of a few degrees can make a large difference in the life of the active device. Thus, a design to achieve a defined operating temperature and verifying the operating channel (or junction in HBT) temperature is an important aspect to be taken into account.
The channel (or junction) temperature is a function of both power dissipation and heat removal. Finally, an important issue is the choice of the heat sink and how is coupled with the chip die.
At *device level* we need the thermal resistance value for thermal design. Thermal modeling of semiconductor can be performed by using numerical techniques based on ANSYS Multiphysics software or by using simple analytic method such as the Cooke model [160] to calculate the thermal resistance (θ) for the transistor. For FETs with gate periphery bigger than 1.5mm measurements of channel temperature with liquid crystal and infrared techniques have shown good agreement with Cooke model. However for gate periphery less than 0.6mm Cooke model over estimates the thermal resistance. Depending of dimension involved we shall work with some of the above mentioned methods.
At *c*ircuit level we shall calculate the heat dissipation budget and structure to take out the heat generated in channel (or junction).
According to the mentioned above this Chapter will be divided in two parts, the first one is related with thermal aspects of the device and the second one deals with thermal circuit design aspects.

8.2 Transistor Thermal Design (Device Level)

Power transistor channel (junction) temperatures not only affects its performance but high channel (junction) temperature degrade the reliability.
The increased temperature causes a degradation of the electron mobility and saturation velocity due to increased lattice scattering. Increased parasitics resistance and reduced channel current result. Based on the FET (or HBT) physical design structure (gate to gate pitch,unit gate width, and FET size, etc), the substrate properties, and the maximum channel temperature, the thermal resistance is calculated.

8.2.1 Thermal Resistance Concept

A transistor has a maximum temperature which cannot be exceeded without destroying the devices or at least shortening its life.
The heat is generated in:

- Bipolars, Under the Emitter (very close to the upper surface of the die).
- FETs, Under the Gate and near drain end.

The ability of a transistor for dissipate heat depends upon a factor called *Thermal Resistance* which may be designed as θ, θ_{th} or R_{th}.
It is defined as follows:

$$Temp_{Rise} = Power_{Dissipated}.Thermal_{Resistance} \tag{8.1}$$

$$\Delta T = PD.\theta \tag{8.2}$$

$$\theta = \frac{\Delta}{P_D}, \circ C/Watt \tag{8.3}$$

Equation 8.2 can be used to calculate the temperature rise at the surface of a chip due to a P_D watts being dissipated, with the bottom of the chip held a constant temperature.
Junction Temperature T_j is given as:

$$T_j = T_A + Temp.Rise - due - to - Heating \tag{8.4}$$

$$T_j = T_A + P_D.\theta \tag{8.5}$$

where T_A is ambient temperature

8.2.2 Calculation of Thermal Resistance

To understand the calculation, in analytical way, of the thermal resistance of a RF power transistor we must first describe the basic mechanisms of heat flow. Depending of the dimensions involved in the transistors two basic flows can be observed, *columnar* and *spreading*. However, in RF power transistors is common that the relationship between dimensions falls in a intermediate zone where heat flow do not behave as a columnar or spreading separately, unless, in a mixed fashion making more difficult the thermal resistance calculation.

8.2.2.1 Columnar Heat Flow

If the thickness of the material is small compared to the lateral dimensions of the device and die (figure 8.1), the heat will flow in a vertical column. The thermal resistance is then calculated as follow:

$$\theta_{columnar} = \frac{F}{K_{TH}.Area} = \frac{F}{K_{TH}.4.C.D} \tag{8.6}$$

Were K_{TH} is the thermal conductivity (this data must be provided by foundry).

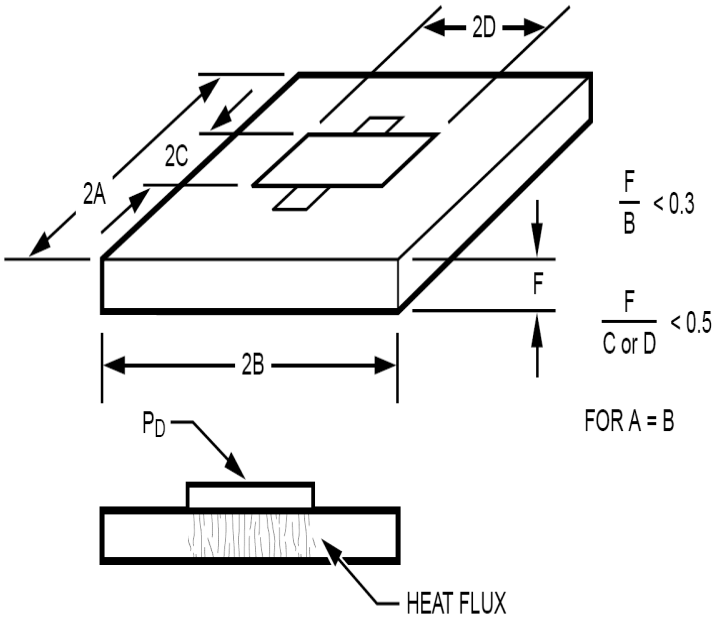


Figure 8.1: Columnar Heat

8.2.2.2 Spreading Heat Flow

The spreading heat flows verifies if the material is thick compared to the device size, and the device dimensions are less than 20% of the side dimensions.
Figure 8.2 illustrates shows how the heat spread out instead of a vertical flow. For this case thermal resistance calculates as follows:

$$\theta_{spread} = \frac{1}{K_{TH}.\pi.\left(\frac{C+D}{2}\right)} \tag{8.7}$$

Note that $(C + D)/2$ is the radius of a circle whose diameter is the average of transistor dimensions.

8.2.3 Single Gate Thermal Resistance Calculation (Between Columnar and Spreading Heat Flow)

As previous mentioned, if the transistors dimensions falls between columnar and spreading forms of heat flow, the thermal resistance must be calculated, evaluating the heat flow using three dimensional Laplace equation like:

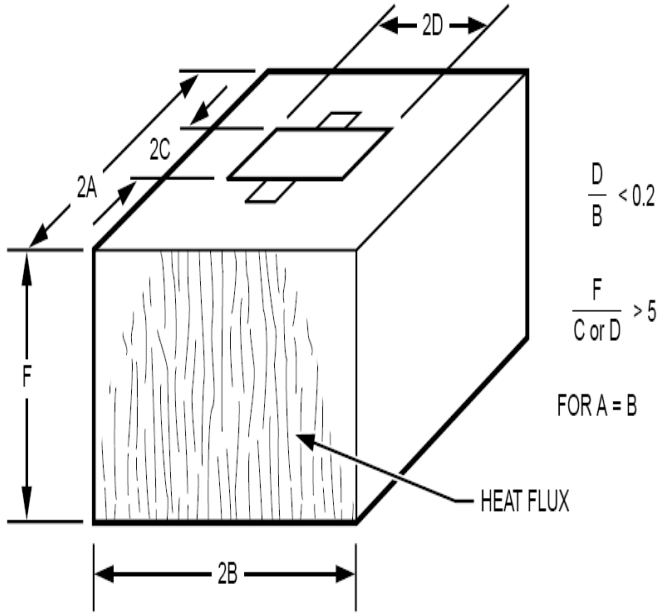


Figure 8.2: Spreading Heat

$$\frac{\partial^2 T}{\partial X^2} + \frac{\partial^2 T}{\partial Y^2} + \frac{\partial^2 T}{\partial Z^2} = 0 \tag{8.8}$$

This equation was solved by Linstead and Surty [272] for several geometries. Anyway for the case of FET the thermal resistance cannot be calculated from [272] since the heat source is a long thin line, not a small rectangle (this thin line is approximated by analogy between fringing capacitance). Using the formula for stripline characteristic impedance given by [273] and the equivalent ideal line as shown by [274], one can derive the following equation for FET thermal resistance:

$$\theta = \frac{1}{2K_{th}W_g}\frac{K(k)}{K(k')} \tag{8.9}$$

where W_g is the unit gate width, K_{th} is the thermal conductivity of the substrate material, and K is the complete elliptical integral of the first kind showed in next equations:

$$k = sech(\pi L'/4h) \tag{8.10}$$

$$k' = tanh(\pi L'/4h) \tag{8.11}$$

$$\tag{8.12}$$

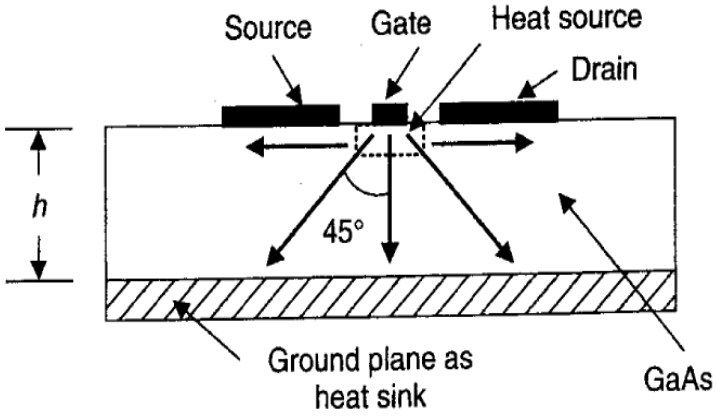


Figure 8.3: Heat Flow in a Single Gate FET

where
$L^{'}$ is the effective gate length and
h is the die thickness
For the details of calculations see [35].

8.2.3.1 Multiple Gate Thermal Resistance Calculation (Between Columnar and Spreading Heat Flow)

As were mentioned in Chapter Combining, to achieve high output RF power is unavoidable to use multifinger transistor, thus, the calculations in this section shall be used for the present feasibility analysis. For the case of multifinger transistors the hat flow is (simplifying) as showed by Figure 8.4:

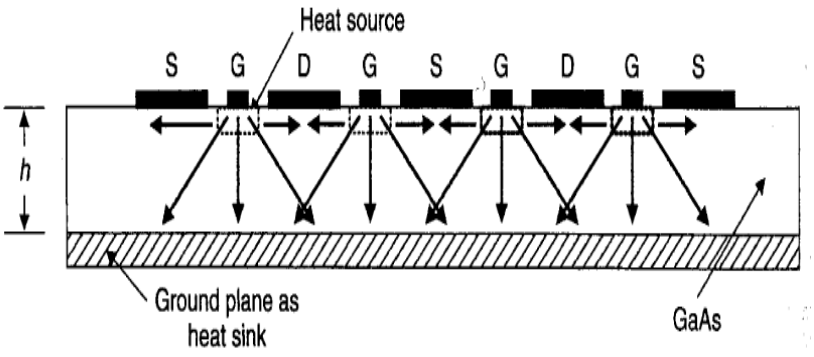


Figure 8.4: Heat Flow in a Multiple Gate FET

A multigate thermal model is derived by treating heat flow in a multigate FET as analogous to the capacitances of multiple coupled transmission lines. The expression for the thermal resistance is given by Cooke [160]:

$$\theta = \frac{n/(ZK_{th})}{\pi\left[\frac{2(n-1)}{ln(M)} - \frac{(n-2)}{ln(P)}\right]}(C^o/W) \tag{8.13}$$

where

$$P = 2\sqrt{\frac{1+sech(\frac{\pi L^{'}}{4h})}{1-sech(\frac{\pi L^{'}}{4h})}} \tag{8.14}$$

$$M = \frac{2\left[cosh\pi(\frac{S+L^{'}}{4h})/cosh\pi(\frac{S-L^{'}}{4h})\right]^{1/2}+1}{\left[cosh\pi(\frac{S+L^{'}}{4h})/cosh\pi(\frac{S-L^{'}}{4h})\right]^{1/2}-1} \tag{8.15}$$

where the thermal conductivity K_{th} is a function of the temperature (should be provide by fondry).
The parameters are defined as follows:
$L^{'}$ = Effective gate length in microns.
S = Gate to gate spacing or pitch in microns.
h = die thickness in microns.
Z = Total Gate periphery in cm.
n = Number of gate fingers.
T = Maximum channel temperatures in C^o.

- **FEASIBILIY HINT:** Calculate Thermal Resistance for different gate-gate pitch for fixed gate length.
- **FEASIBILIY HINT:** Calculate Thermal Resistance versus number of gates for a fixed gate length.

8.2.4 Decision Making on Thermal Resistance

NOTE: The decision making at present work is driven primarily by reliability aspects leaving so far as a secondary matter the aspects related with die size (costs), therefore, the study of the thermal resistance of the transistor (namely, its ability to extract heat from its channel or junction to outside the die) is a central aspect of this feasibility study.

From the design's perspective the calculation of the thermal resistance shall be used in next section to complete the *thermal budget*. The value obtained in this section, which is highly dependent of the transistor fingers structure, also could be re calculated iteratively (if needed) according to the results obtained in the study of the transistor structure toward maximizing the output power. The result

presented shall be based mainly on the following criteria:

Primary Criteria:

1. Thermal Resistance (Reliability).
2. Life Cycle in Function of Operating Temperature (Reliability).

To the end of this feasibility study a comparative table of above mentioned criteria shall be delivered. This table must present a comparison of each criteria (by foundry process) and a must contain a weighting function of each criteria to eases the decision making. The weighting of criteria would be modified in due course if required by CONAE.

8.3 Pulsed Thermal Resistance (Pulsed Application)

Up to now when we refer to thermal resistance calculation we assumed that the power applied active device is continuous. However there are applications where the power applied is discontinuous, for example in radar systems where the same antenna transmit energy for a short period of time a must stay-off transmitting for a comparative longer period of time. In those cases a new considerations related to thermal resistance must be taken into account.
Under pulsed operation the die behaves with a thermal time constant, namely, the temperature do not raises instantaneously, but has a rise and fall time equivalent to an equivalent capacitive-resistive circuit . Semiconductor temperature as a function of time can be given as:

$$T_j = P_D\theta \left[\frac{4}{\pi^{3/2}}\right] \left[\frac{t}{\tau}\right]^{1/2} + T_A \tag{8.16}$$

for $t < \tau$, $\tau = thermaltimeconstant$ and $t = time$. Note that, the temperature is proportional to the square root of time, thus, the RC analog is not exact (see [35]) although this approximation is useful in most cases.

The thermal time constant can be estimated by:

$$\tau = \left[\frac{2h}{\pi}\right]^2 \left[\frac{\rho C}{K_{th}}\right] \tag{8.17}$$

where h is the die thickness.
ρ is the density of semiconductor.
K_{th} is the thermal conductivity.
C is the heat in the semiconductor.

The thermal design of pulsed transistors is less stringent than continuous wave operation transistors. Under pulsed operation the reliability and life cycle of the active devices are enhanced.
The operation under pulsed condition do not improve the output power significantly because the output power is limited by the output peak current and the maximum output breakdown voltage. However depending on the pulse duration respect to its repetition frequency (duty cycle) and the thermal time constant of the devices the case temperature can be raised without exceeding the channel temperature. For example a GaAs MMIC pulsed below 30 μsec have about 0.5 to 1 dB higher output power and 3-5 % higher PAE than in continuous operation [24].

When a power transistor is operating under pulsed conditions, the channel rise after applying DC power is approximately given by nex expression [268]:

$$T_{ch} = P_D R_{th} \left[1 - \frac{8}{\pi^2} \sum_{n=1,2,3..}^{\infty} \left(e^{-n^2 t/\tau} / n^2 \right) \right] + T_a \tag{8.18}$$

where τ is the thermal time constant, P_D is the net power dissipated in the device, R_{th} is the thermal resistance, and t is the time after DC power is applied to the device. For $t < \tau$, an approximate expression for T_{ch} may be written as [35]:

$$T_{ch} = P_D R_{th} \left(\frac{4}{\pi^{3/2}} \right) \left(\frac{t}{\tau}^{1-2} \right) + T_a \tag{8.19}$$

the approximated expression for τ was given in equation 8.17.
For *l*ong pulses i.e., pulse length greater than 2τ, the channel temperature will correspond to continuous operation. When pulsed operation, the channel temperature after t_0 second of pulsed power is given by:

$$T_{ch} = P_D R_{th} \left(\frac{t - t_0}{2\tau} \right)^{1/2} + T_a \tag{8.20}$$

If $t - t_0$ correspond to the pulse width the maximum channel temperature is:

$$T_{max} = P_d R_{th} \left(\frac{PulseWidth}{2\tau} \right)^{1/2} + t_a \tag{8.21}$$

and occurs when the pulse is on, after that the die starts to cool down.

- **FEASIBILITY HINT:** Find out (foundry data) or calculate thermal time constant.
- **FEASIBILITY HINT:** Compare thermal time constant of process with pulse specification from transponder's standard studied in Chapter 1.
- **FEASIBILITY HINT:** Calculate maximum expected channel temperature (worst case).

8.3.1 Decision Making on Pulsed Thermal Resistance

NOTE: The decision making at present work is driven primarily by reliability aspects leaving so far as a secondary matter the aspects related with die size (costs), therefore, the study of the life of the transistor versus its channel (junction) temperature is a central aspect of this feasibility study.
The result presented shall be based mainly on the following criteria:

Primary Criteria:

1. Thermal time constant (Reliability).
2. Maximum channel temperature for worst case of duty cycle (Reliability).
3. Life Time versus channel temperature(Reliability).

To the end of this feasibility study a comparative table of above mentioned criteria shall be delivered. This table must present a comparison of each criteria (by foundry process).

8.4 Measurement of Thermal Resistance and Channel (Junction) Temperature

It is highly recommendable to measure in laboratory the thermal resistance and/or the channel (junction) temperature to verify/validate the analytic results. To do that, there are several laboratory equipments to make measurements depending on the method to be used.

See for example [35], [275], [24] and [276]. Below is a brief list of the methods under consideration:

8.4.1 Infrared Image Measurement

The scope of use and an analysis of its advantages and disadvantages, including recommendations about laboratory equipment, are presented in Chapter 5 (Third Deliverable Document).
Refers in advance to [277] and [278] if necessary. The next two methods were discarded a priori since do not match the feasibility requirements, anyway we present the reference material from where we develop the previous conclusion.

8.4.2 Liquid Crystal Measurement

For details refers to [279].

8.4.3 Electrical Measurement

For details refers to [280].

8.5 Device Life vs Channel (Junction) Temperature

As mentioned before a major factor affecting the operating junction is how the power is applied and dissipated by the device either the power being pulsed or continuous.

The life of an amplifier is largely determined by the life of its active devices (mainly power devices), which in turn is determined by physical phenomena such as a metal migration, dopant diffusion, or other modifications of the device characteristics. These phenomena are critically dependent on temperature. One of the most useful models relating temperature to the speed of a physical or chemical reaction is the Arrhenius model which express the rate of change, r, as:

$$r = Ae^{-\frac{E_A}{KT}} \tag{8.22}$$

where A is a constant, E_A is an *activation energy* characteristic of the specific process (see for example [281]), K is the Boltzman constant $[8.617 * 10^5(eV/K)]$ and T is the absolute temperature in K. Experience has shown that 8.22 models quite well many of the phenomena which lead to failure in an electronic component. Accordingly, we expect the life of component l, to be inversely proportional to r. Then its relation to temperature is given by:

$$l = Be^{\frac{E_A}{KT}} \tag{8.23}$$

where B is a constant. It is also useful to define a relative life time, by making reference to the component's life, l_0, at a normalized temperature T_0. Based on 8.23

$$l_0 = Be^{\frac{E_A}{kT_0}} \tag{8.24}$$

thus the relative life time is:

$$\lambda = \frac{l}{l_0} = e^{\frac{E_A}{K}\left(\frac{1}{T}-\frac{1}{T_0}\right)} \tag{8.25}$$

To understand the concept of relative life time versus temperature we may refers to Figure 8.5. In this example can be observed how a typical FET operating at 100C (reference given by the foundry) of channel temperature (25C case temperature). For this device the primary failure mechanism is is the gate metal inter diffusion produced at given activation energy [281]. Is interesting to note the high

slope of the curve: for example the life time decreases by a factor of 10 for a temperature increased only 30C and decrease by a factor of 2 for an increase of 8C. Conversely, similar increases of life time are obtained for similar decreases in channel temperature. Clearly a few degree's improvement can make a very substantial change in the life of the device.

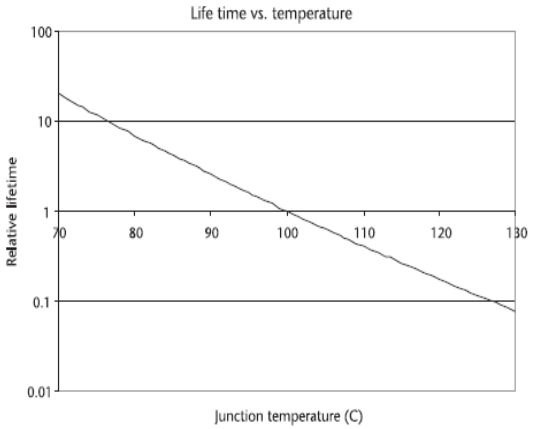


Figure 8.5: Relative Life Time versus Junction Temp. for a given Activation Energy

- **FEASIBILITY HINT:** Obtain reference life time of device at given temperature.
- **FEASIBILITY HINT:** Calculate relative life time for a given channel temperature. This temperature shall be calculated iteratively in function of other feasibility aspects (size , power, efficiency, etc.,).

8.5.1 Decision Making on Life Time versus Temperature

NOTE: The decision making at present work is driven primarily by reliability aspects leaving so far as a secondary matter the aspects related with die size (costs), therefore, the study of the life of the transistor versus its channel (junction) temperature is a central aspect of this feasibility study.
The result presented shall be based mainly on the following criteria:

Primary Criteria:

1. Reference Life Time (Reliability).
2. Relative Life Time at Given Operating Temperature (Reliability).

To the end of this feasibility study a comparative table of above mentioned criteria shall be delivered. This table must present a comparison of each criteria (by foundry process) and a must contain a

weighting function of each criteria to eases the decision making. The weighting of criteria would be modified in due course if required by CONAE.

8.6 Amplifier Thermal Design (Circuit Level)

Once thermal resistance and channel (junction) temperature are determined a further step is required to complete the *thermal budget* of the complete design, namely, the die attached to some thermal conducting material (metal) and how this support (package) is connected to a heat sink completing the heat transferring cycle from the channel (junction) to the operating ambient.

To model the heat transference chain we follow the same approach presented before, each material that connect to the die is defined by its thermal resistance. Then the thermal resistance from junction to package is R_{JC}(Junction-Case), the thermal resistance from package to silicone grease R_{CS}(Case-Silicone) and the heat sink has a thermal resistance R_{SA}(Sink-Ambient) (see figures 8.6 and 8.7). Of course this is a simplified model but allow us to understand the main mechanism.

Between die and case may exist several films of different materials:die solder attachment, epoxy, etc. The structure of die attachment must be provided by foundry or must be investigated during the course of this work. In due time different thermal constants shall be outlined to complete the thermal study.

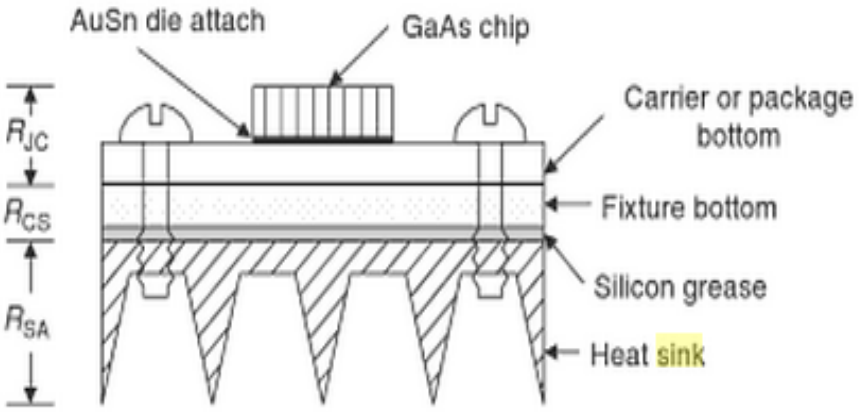


Figure 8.6: Chip attachment to the heat sink (From [24])

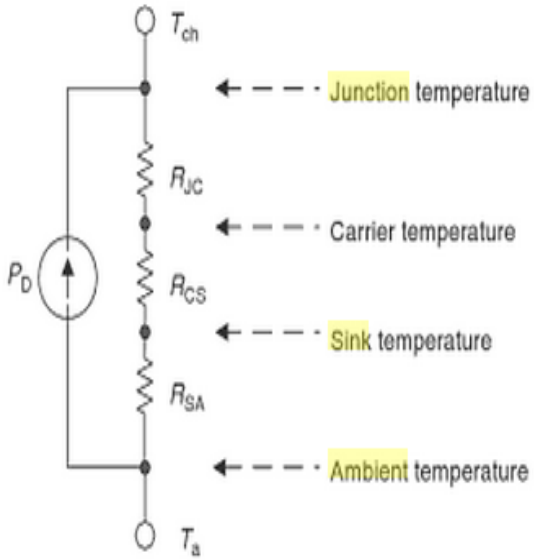


Figure 8.7: Thermal equivalent model (From [24])

Following the notation described before the total power dissipation(P_D) in the active device can be calculated as:

$$P_D = \frac{T_{ch} - T_a}{R_{JC} + R_{CS} + R_{SA}} \tag{8.26}$$

where
T_{ch} is the channel temperature.
T_a is the ambient temperature.

and the channel temperature is defined as follow:

$$T_{ch} = (R_{JC} + R_{CS}R_{SA}) + T_a \tag{8.27}$$

Power amplifiers are generally soldered to carriers (case) using 80-20 gold-tin preforms, which are cut from sheets. The carrier material can be cooper. The higher the material thermal conductivity the higher the price. All cases (packages) are plated with nickel and gold.

- **FEASIBILITY HINT:** Evaluate the mechanical bond structure from die to case.
- **FEASIBILITY HINT:** Find out (foundry data) or calculate the thermal resistance of the materials involved in previous structure.

- **FEASIBILITY HINT:** Calculate the required thermal resistance of heat sink to evaluate its size feasibility.

8.6.1 Decision Making on Amplifier Thermal Design

The selection of a heat transfer structure (die to heat sink) will be outlined. The study shall based mainly on the following criteria:

Primary Criteria:

1. Thermal Budget and Management (Reliability).
2. Die Attaching material properties and structure (Reliability).
3. Heat Sink Minimum Size(Reliability).

To the end of this feasibility study a comparative table of above mentioned criteria shall be delivered. This table must present a comparison of each criteria (by foundry process and packaging technology) and a must contain a weighting function of each criteria to eases the decision making. The weighting of criteria would be modified in due course if required by CONAE.

Chapter 9

Device Scaling, Device Paralleling, Device Series and Power Combining

This chapter presents a basic theory formulation for device scaling, paralleling and power combining techniques, including equations, figures and references. The main intention is to develop a minimum self contained material of the subject under study that serves of guidance during the feasibility study and also be useful for discussion template between involved organisms (IIIE -CONAE).
The material presented in this chapter is thought to support concepts related to the *design strategy* aspects presented in chapter 2 (First Deliverable Document).

For simplicity not all equations a figures are included, when considered references are given to deepen understanding. The references are not necessarily the state of art in particular case, unless, they are the most relevant work even they were published long time ago. The state of art of the subject studied here is presented in chapter 3 (Second Deliverable Document).

9.1 Introduction

In microwave power transistors, with increasing frequency, the power output from a single transistor decreases rapidly. In many applications microwave power levels are required that far exceed the capability of any single unit cell device or amplifier. Is therefore desirable to extend the power level on an amplifier by utilizing device scaling, paralleling or power combining techniques.
Although there are fundamental limitations to the power that can be generated from a single transistor, the achievable power levels can be increased significantly by combining a number of devices operating coherently or by accumulating the power form a number of discrete devices. This may be done in two different ways: by either combining power at the *device level* or at the *circuit level*, see figure 9.1.

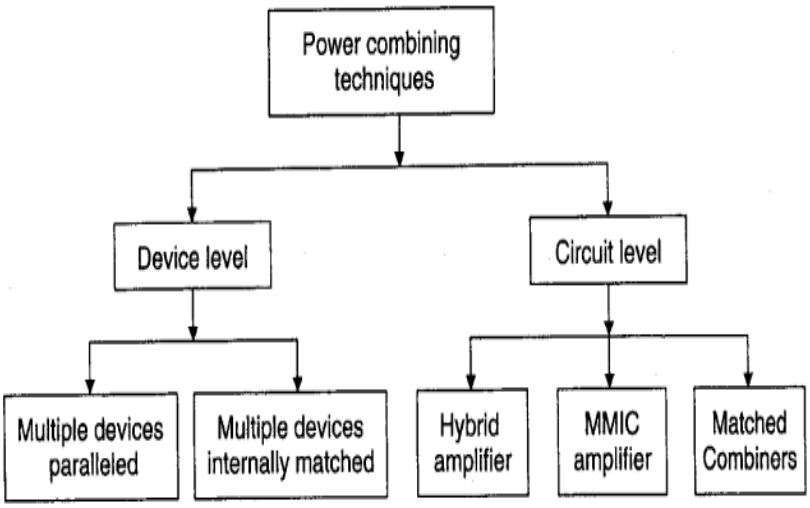


Figure 9.1: Device and Circuit Power Combining Techniques

9.2 Device Level

9.2.1 Device Scaling

The theory presented below is mainly related to FET devices but also applies to HBT devices.
The first step towards increasing the output power capability is to attempt to scale the device to increase the output current or voltage capability increasing its size (if possible both at same time). Nevertheless, such an option is related to the availability of an affordable monolithic technology. Moreover the scaling properties of a given technology are strictly valid for moderate scaling only. For the same total gate or emitter periphery, in fact, while the output power remains almost constant (at given frequency), the large signal gain decreases with unit gate width, thus also affecting the PAE performance.
Figure 9.2 shows two ways to increase the gate periphery in a FET device:

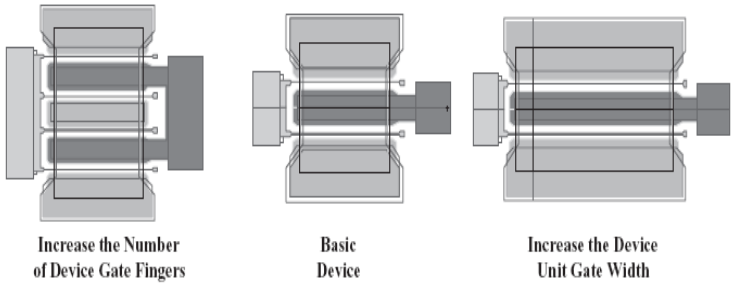


Figure 9.2: Increasing FET maximum current. Left: Increasing Gate fingers. Right: Increasing Gate Width

Moreover, an increase in device periphery actually increases also device parasitics effects, leading to a reduction in gain and operating frequency [282]. From the thermal management point of view, scaling up the device periphery implies an increase in dissipated power, resulting in a increased device junction or channel operating temperature, thus implying detrimental effects both in device performance and reliability (life cycle). Junction or emitter temperature parameter is a rough limit in the degrees of freedom of device scaling, making mandatory the use of device paralleling or power combiner techniques when both high power and high frequency are required.
NOTE: For the microwave powers involved in this feasibility study it is assumed that a single device with a multi finger structure will be mandatory.

As an example, if a MMIC process technology (based on FET active devices) has a power density of $\delta_p = 1W/mm$ and we need to deliver $10W$ of output power the device must be scaled as follow:

$$T_{gate} = \frac{P_{out}}{\delta_p} = \frac{10W}{1W/mm} = 10mm \tag{9.1}$$

where T_{gate} is the total gate periphery. If a simple 10mm gate periphery is not available or it is not suitable for the application, the number of devices to be combined to fulfill the required output power level has to be determined either in paralleling devices or power combining techniques (next sections).
It is customary that the devices scaling options provided by the foundry results in discrete values, for example, $T_{gate} = 1mm$, $T_{gate} = 1.5mm$, $T_{gate} = 2mm$ and so on, then if available the selection shall be done on the device with discrete periphery value that equals or surpasses the power requirement.

- **FEASIBILITY HINT:** Scaling shall be done following foundry recommendations (layout rules). Manual scaling (although possible) will be out of scope of this feasibility study.
- **FEASIBILITY HINT:** Calculation of maximum junction temperature as function of reliability specification based on foundry process data.

- **FEASIBILITY HINT:** Phase error along the individual gate fingers are produced when their dimensions approach a significant fraction of wavelength of the signal traveling down them.
- **FEASIBILITY HINT:** Phase error between gate finger are produced when device become large (many fingers) and the distance between the central feeding track is different from central fingers than for peripheral fingers.
- **FEASIBILITY HINT:** Thermal calculation must be done over central fingers which are the hottest one, see thermal model presented in [160].

9.2.2 Decision Making on Device Scaling

NOTE: The decision making at present work is driven primarily by reliability aspects leaving so far as a secondary matter the aspects related with die size (costs) or design engineering costs (device complexity). The selection of a power device size shall be based mainly on the following criteria:

Primary Criteria:

1. Thermal Budget and Management (Reliability).
2. Device Efficiency (Reliability).
3. Resistance to VSWR (Reliability).
4. Radiation Resistance (Reliability)

Secondary Criteria:

1. Die Size (Cost).
2. Design Complexity (Cost).
3. Input & Output Impedance (Cost).

NOTE: Of course, in above criteria, is taken for granted that cut-off frequency and gain are preserved above required values during scaling calculations.

The deliverable at this point shall present an active device calculation (by foundry process) with its maximum possible size (output power).
A comparative table of active devices ordered by the above criteria shall be delivered. This table must present a comparison by each criteria (by foundry process) and a must contain a weighting function of each criteria to eases the decision making. The weighting of criteria would be modified in due course if required by CONAE.

9.2.3 Multiple Device Paralleled

If maximum size (transistor cell) obtained in previous section (highly restricted by frequency and temperature) do not complies with the output power requirements, paralleling of several cells must be considered.
Devices paralleling is accomplished by clustering the devices in a region whose extent is small compared with a wavelength, and the number of devices that can be combined efficiently is limited. We consider here the on-chip device paralleling bonded individually to a common rail connection see Figure 9.3.
Device in Figure 9.3 is a commercial pHEMT available in 2,4 and cell configurations.

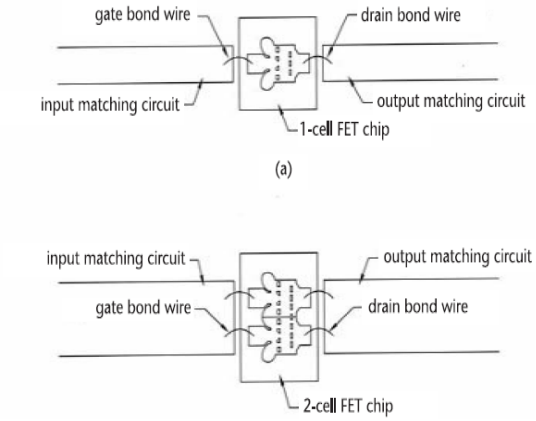


Figure 9.3: One and Two transistor cell bonded to a common connection (From [25])

To evaluate what happens when cell are paralleled we must consider that the bond wires used to interconnect cells acts now as a part of input an output impedances. They are modeled as inductances and when connected do not scales linearly since mutual coupling effects appears.
The inductances of gate and drain (source is commonly connected through source bias) bond must be calculated if an evaluation of cut-off frequency is required. Calculation of characteristic impedances of the bond wires can be done in analytical way using equations presented in [51]. The total impedance of bond wire arrangement can be found in [276]. Concluding, since the paralleling cell do not scale linearly the parasitics the increase of power in inevitably at expense of bandwidth (or cut-off frequency). Here we present the bond wire effect being the most important one , there are another parasitics to be taken into account.

In theory, this approach is only really useful at low RF frequencies (below 3GHz), where the phase difference between the device feeds is a sufficiently small fraction of the transmission wavelength . This technique is mainly used with the purpose of a better thermal management in a MMIC using small transistors.
As an example, figure 9.4 shows a commercial LDMOS power transistor designed with several LDMOS cell transistors arranged in parallel.

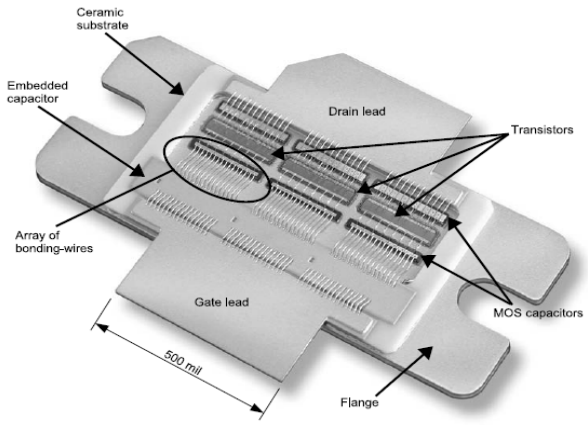


Figure 9.4: Freescale LDMOS Power Transistor (From [26])

In next figure we can observe a detailed view of the LDMOS die with 80 fingers to increase gate periphery which is a constitutive part of the transistor showed in Figure 9.4. In this figure can be observed that the power transistor is composed by three dies like showed in 9.5.

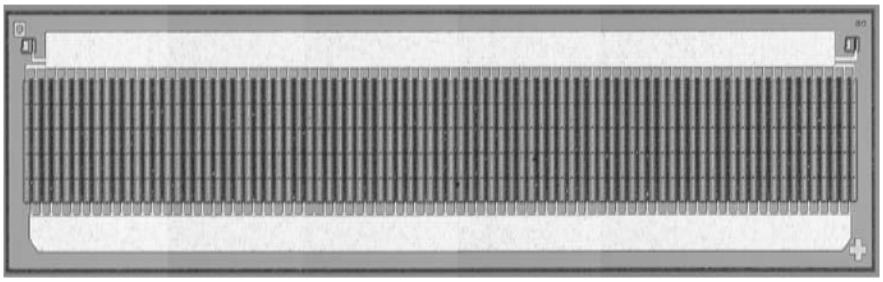


Figure 9.5: Freescale LDMOS single transistor die with 80 fingers gate (From [26])

- **FEASIBILITY HINT:** Calculate relative bandwidth and bond wire inductances versus number of wires (parallel cells).

9.2.3.1 Multiple Internally Matched (Parallel Matching)

Parallel matching [283] is a technique to fit the best (optimum) output and input impedance of a cluster of parallel transistors prior to the paralleling of themselves. For example (we parallel for transistor cell), if instead of match each transistor cell to 50Ω we adapt ha matching network to $4 * 50\Omega = 200\Omega$. In that way optimum lumped or distributed element of matching networks are calculated. This procedure should lead to a more compact (size) and less lossy matching network than using separate matching

individual transistor cells. More details will be presented in chapter *matching networks*.

9.2.4 Decision Making on Device Paralleling

NOTE: The decision making at present work is driven primarily by reliability aspects leaving so far as a secondary matter the aspects related with die size (costs) or design engineering costs (circuit complexity).
The selection of a power device size shall be based mainly on the following criteria:

Primary Criteria:

1. Thermal Budget and Management (Reliability).
2. Device Efficiency (Reliability).
3. Resistance to VSWR (Reliability).
4. Radiation Resistance (Reliability)

Secondary Criteria:

1. Parallel cells Die Size (Cost).
2. Design Complexity (Cost).
3. Input & Output Impedance (Cost).

The deliverable at this point shall present a calculations in terms of wavelength for paralleling transistors cells (defined in previous section) for each foundry process under study. The results shall be presented in a table to allow an easy comparison between foundry process and also to determine if feasible the implementation of paralleling or must be considered the use of power combining structures either, on-chip or off-chip (next section).

9.2.5 Multiple Device in Series

For active devices with output breakdown voltage below 6V it is very difficult to obtain high output levels of microwave power, even when paralleling or combining techniques were used. One method to overcome the low breakdown voltage limitation is to arrange several deices in series making that each devices support only a fraction of the output voltage. There are several trade-offs playing a role is this type of

designs and there is no clear limit to define when is beneficial to use series technique instead of parallel or combining technique. Anyway we present here the basic aspects needed to better decision making.

When devices are connected in series for DC bias (see Figure 9.6) the RF input and output is stetted in parallel ([284], [285]), the last limits the number of devices since we can not lowers the impedances below certain threshold were the matching network become very complex to implement.

Recently, an improved version [286] of the topology under consideration was presented which makes

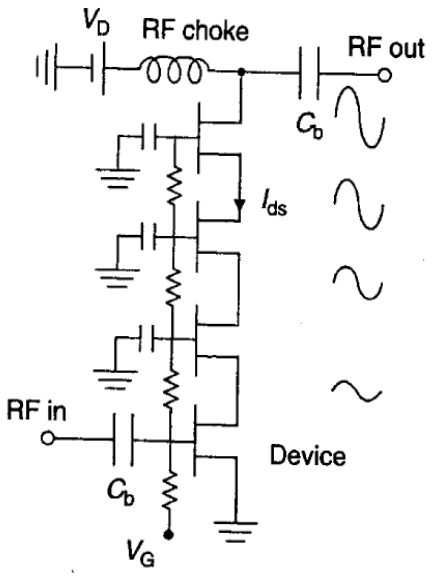


Figure 9.6: Configuration of four FETs in series for high voltage operation

that both, DC and RF path, are in parallel which makes that V_{Out} and Z_{Out} be:

$$V_{Out} = N.V_{Out_{Device}} \tag{9.2}$$

and,

$$Z_{Out} = N.V_{Out_{Device}}/I_{ds} \tag{9.3}$$

9.2.6 Decision Making on Device in Series

NOTE: The decision making at present work is driven primarily by reliability aspects leaving so far as a secondary matter the aspects related with die size (foundry costs) or design circuit complexity (engineering costs).

The selection of a power series configuration shall be based mainly on the following criteria:

Primary Criteria:

1. Thermal Budget and Management (Reliability).
2. Resistance to VSWR (Reliability).
3. Radiation Resistance (Reliability)

Secondary Criteria:

1. Series cells Die Size (Cost).
2. Design Complexity (Cost).
3. Input & Output Impedance (Cost).

The deliverable at this point shall present a calculations in erms of number of devices, impedances and sizes involved for each foundry process under study. The results shall be presented in a table to allow an easy comparison between foundry process and also to determine if feasible the implementation of series or must be considered the use of power combining structures either, on-chip or off-chip (next section).

9.3 Circuit Level

Device level combining is generally limited due to the number of transistors that can be combined and effectively matched on a small area. High power transistors are also matched and combined as an amplifier using the hybrid IC technique. However, monolithic power amplifier have shown great promise as an alternative to chip combining. These amplifiers have built in power devices and matching networks with considerably advantages of small size, light weight (very important in space applications), low cost and fully matched circuits.
From now, when we refer to a circuit circuit level power combining technique is referring to a matched power splitters and combiners.
There are two main groups of splitting /combining techniques, *resonant cavity* and *non resonant cavity* (see figure 9.7).

The first ones, (out of the scope of this feasibility study), uses waveguide components with low loss and high combining efficiency.
The second ones, (falls inside the scope of this feasibility study) are based mainly in planar micro strips devices that allow the power splitting and combining. Among all *non resonant* techniques there are two main categories (See Fig. 9.7):

- Those that combine the output power of N devices in a single step, known as *N-way combiners*.
- Those that combine the output power of N devices in a tree or chain combining structures, known as *c*orporate combiners.

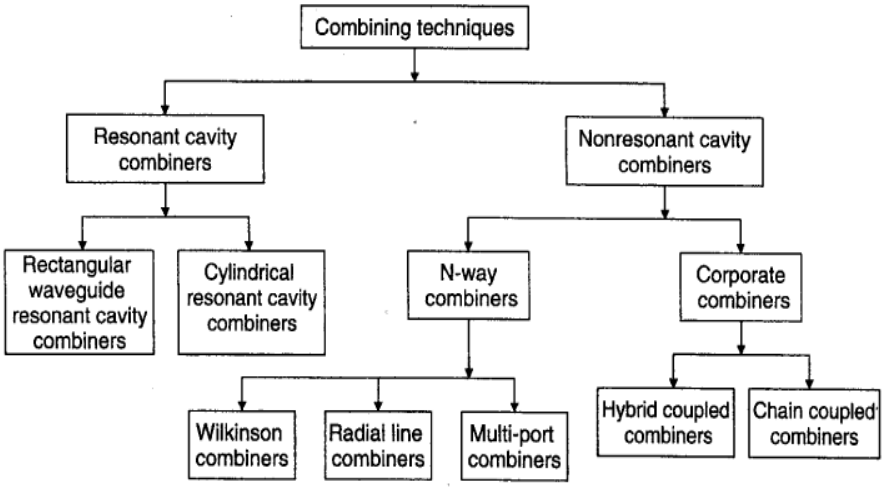


Figure 9.7: Different Circuit Combining Techniques Using Power Combiners

9.3.1 N-Way Combiners

N-way combining structures are simpler than corporate combiners as they avoid the use of several stages, thus making it possible to achieve high-efficiency combining [276], [24] & [287].
The scope of this work deals with *non-resonant N-way combiners*, even they have more insertion loss and poorer efficiency than resonant. The reason is that this ones can be developed in a MMIC microstrip planar and coplanar circuit meanwhile the resonant ones are not applicable for this technology.
Figure 9.8 resumes the concept of how the power is splitted and added in a tree configuration. There are three main types of N-way combiners , although a mixed combination of them can be found in MMIC implementations¿ The most used are listed below:

- bus bar combiner.
- Wilkinson Combiner.
- Radial Combiner.
- planar multi-port.

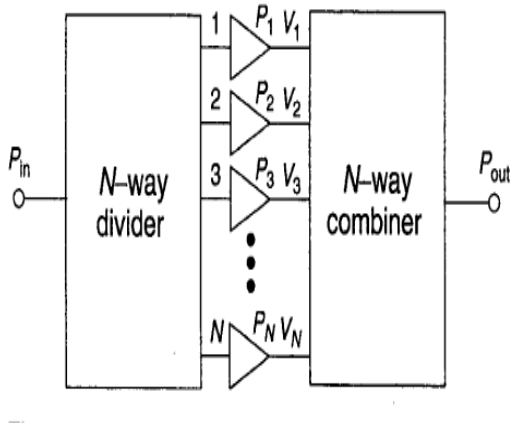


Figure 9.8: N-Way Power Combining Scheme

9.3.1.0.1 N-Way Bus Bar Bus bar combiner is used in MMIC amplifier design to combine very large number of devices (2^N) in a very compact way , see refs [288], [180], [283], [289]. The scheme of bus bar is showed in Figure 9.9.

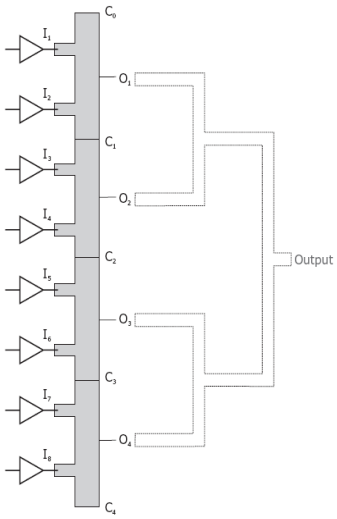


Figure 9.9: Bus Bar Combining Structure

The bus bar is based on a wide metal track placed immediately across the devices outputs [283]. The power delivered from a single device is combined in the output tree structure, this combination is usually based on Wilkinson power combiner.

One big advantage of this structure is related to the possibility of using the same metal strip to feed DC to all the devices at the output. The structure operates under the assumption of equal phase and amplitude of the excitation provided by the power sources. The separation between input ports should be small as compared to the wavelength of the highest operating frequency thus avoiding odd mode

oscillations.
In due course of the feasibility study we shall refers to [288], [180], [283], [289] [290], [291], [287], [276], [24], [261] and [292], for detailed design aspects of this structure.

9.3.1.0.2 N-Way Wilkinson Combiner One of the most popular and widely power combining structure was proposed by E. J. Wilkinson [293]. Originally proposed as an N-way divider for planar implementation, it is most useful with $N = 2$, since for $N > 2$ implies a three dimensional structure requiring a significant modification to be introduced in a planar circuit.
The basic scheme for a N-Way divider is shown in Figure 9.16:

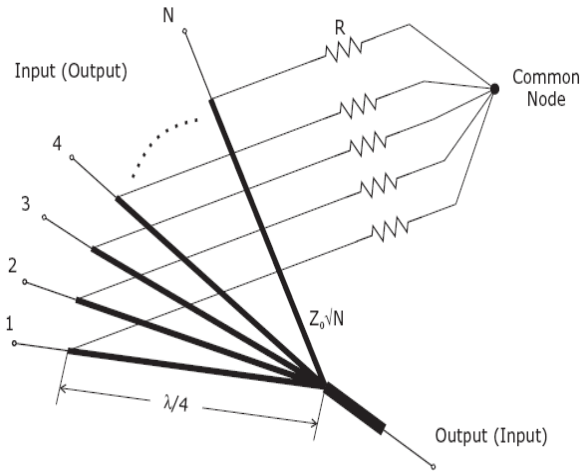


Figure 9.10: N-Way Wilkinson Divider/Combiner

The main assumption of this circuit is that the power is divided in equal parts and input output ports have the same characteristic impedance Z_0. The transmission line impedance in each dividing (combining) branch is $Z_0.\sqrt{N}$, where N is the number of division (summing) branches. Each of the output ports is connected to a floating node by a balancing resistor $R = Z_0$, mandatory to provide isolation among ports.
It is clear from Figure 9.16 that for $N > 2$ is impossible to implement the circuit in a planar technology. Although, there are N-way implementation in 3D multilayer LTCC substrates [87], but this technology falls off outside the possibility of available foundry process (we do not discard this possibility in the future). On the other hand, several approaches does exist that allow the N-Way to be implemented in a planar technology. See next paragraph.

The main advantages of N-way Wilkinson combiners are: low loss, moderate bandwidth and good amplitude an phase balance. However, its major disadvantages for power applications the floating

star-point isolation resistors. This resistor requires a nonplanar crossover configuration, which limit the power handling capability.

9.3.1.0.3 N-Way Wilkinson Combiner with air bridges For RF and low microwave the planar solution for n-way Wilkinson disadvantage is based on the introduction of air bridges realized through bonding wire connections [24], (figure 9.11). The details of this implementation can be found in [294].

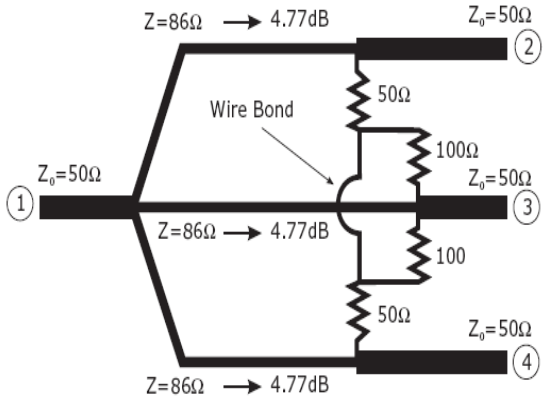


Figure 9.11: N-Way Wilkinson using air bridge bonding wire

9.3.1.0.4 N-way Simplified Wilkinson Combiner Previous mentioned drawbacks also can be solved using a simplified version of n-way Wilkinson combiner like proposed by [295] (figure 9.12), with a combining efficiency of 90%, which shows good promise for MMICs applications.

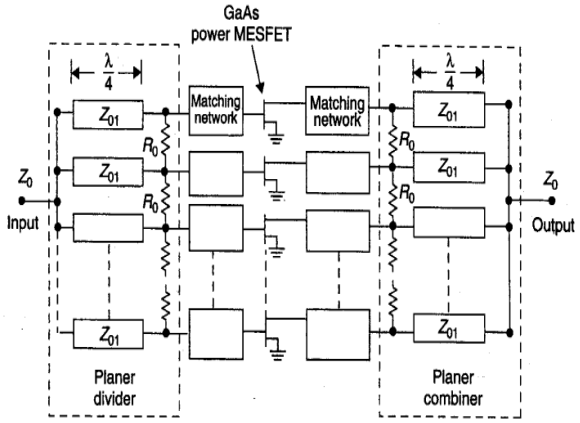


Figure 9.12: Modified N-Way Wilkinson Divider Combiner

9.3.1.0.5 N-Way Radial Wilkinson Combiner Is a modified version [296] of N-way Wilkinson who represents one of the most effective approach to implement a planar version of N-way Wilkinson circuit (figure 9.13).

Even though that radial line combiner has low insertion loss, good isolation and phase symmetry its application is impractical in foundry process under study due to its three dimensional structure. Thus, we consider this circuit *out of the scope* of this work, being introduced at this paragraph only for review purposes. In these structures the isolating resistor are not connected to the floating node, but each adjacent transmission line is connected to each other. For details refers to [297].

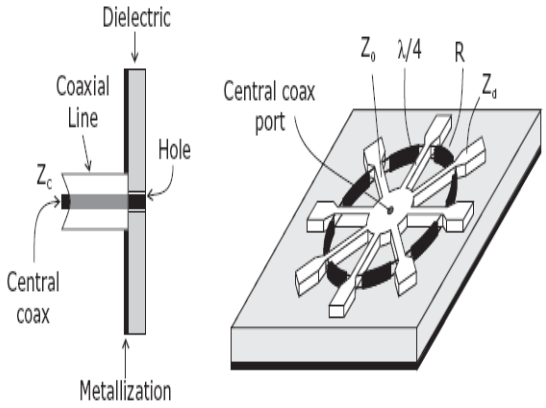


Figure 9.13: Radial N-Way Wilkinson Combiner

9.3.1.0.6 N-Way Planar Combiner The planar N-way combiner/divider, (figure 9.14), requires $(N-1)N$ quarter wave section for maximum isolation an thus is very large in size compared with previous mentioned Wilkinson schemes. Details of this scheme can be found in [298]

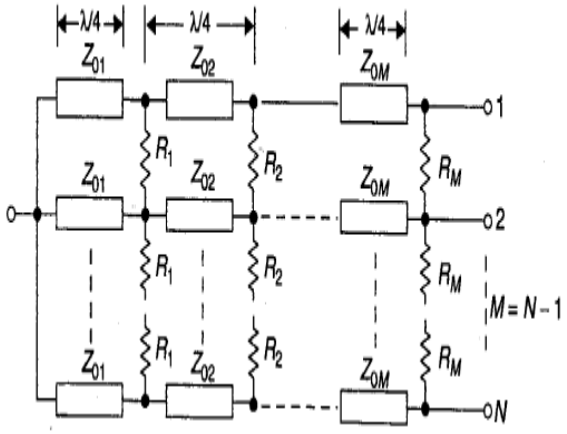


Figure 9.14: N-Way planar divider-combiner

9.3.2 Corporate Combiners

A corporate structure (or tree) structure for combining two-way adders is shown in figure 9.15. These two way adders can be implemented with Wilkinson, Hybrids or the Rat Race Hybrid. The loss in the adders limits the combining efficiency of the corporate structure versus the number of devices for various loss-per-adder values. The number of devices combined in this way is binary. There are corporate solutions based on tree architectures or serial combining (traveling waves).
Two way adders are can be done with: two way Wilkinson, directional couplers and hybrids. Among the two way adders , the Lange Couplers are preferred because of its good bandwidth and high isolation. Corporate structures are impractical (due to efficiency loss) beyond a four way combiner.

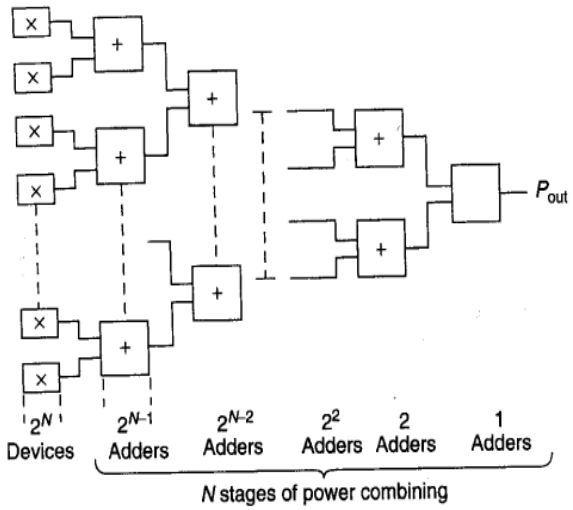


Figure 9.15: Corporate Combining Structure

FEASIBILITY HINT: Calculate the combining Efficiency in terms of number of combined devices and with a specific insertion loss per adder.

9.3.2.0.7 Two way Wilkinson Corporate Structure The Wilkinson Corporate (with building blocks of $M = 2$) is preferred for practical application due to its simplicity, the building blocks ensures an isolation of at least 20dB and operating bandwidth of 20%.

9.3.2.0.8 Four ports Hybrid Corporate Structure Compared with Wilkinson, the hybrids have better isolation but with the drawbacks that must properly terminated at system impedance to ensure good matching condition. Also phase shift must be careful designed and evaluated to avoid phase unbalance between adders. The structure is depicted in Figure 9.17

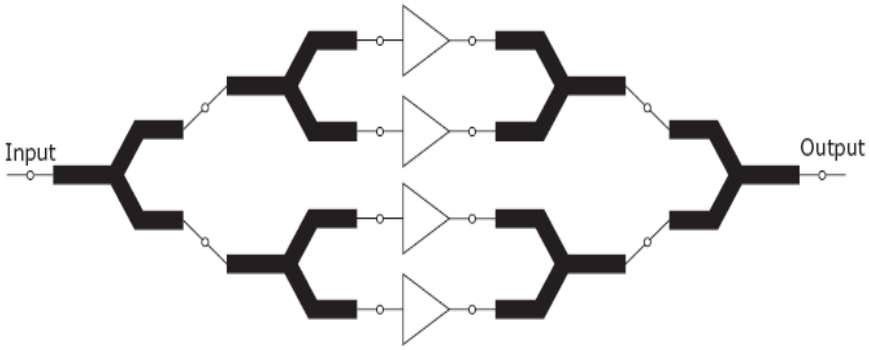


Figure 9.16: Two way Wilkinson Corporate Structure

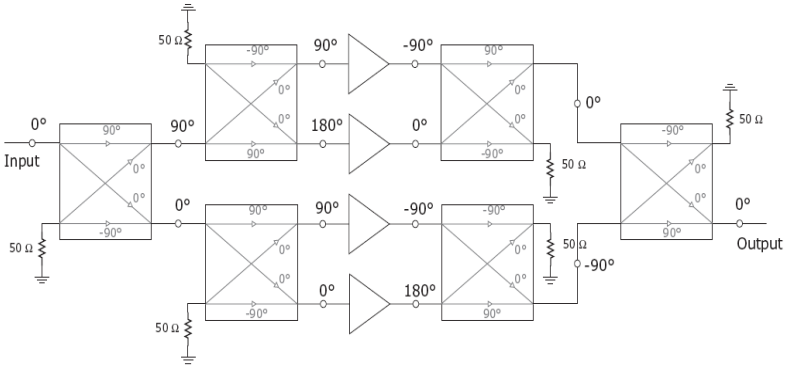


Figure 9.17: Four Ports Hybrid Corporate Structure

9.3.2.0.9 Mixed Two-way Wilkinson/Hybrid Corporate Structure The mixed solution (Figure 9.18) can be adopted where the input and output 3dB hybrids are adopted to improve the overall structure VSWR, while two way Wilkinson splitters/combiners are selected for internal building blocks. In both cases, using hybrids, Lange coupler is recommended since requires less chip area.

- **FEASIBILITY HINT:** Calculate the combining Efficiency in terms of number of combined devices and with a specific insertion loss per adder for each MMIC process.

9.3.3 Serial, Chain or Traveling Wave Combiners

A corporate combiner can also be realized using hybrids in a chain (or serial) configuration [299], [300](see Figure 9.19). In such configuration, to realize a N-way combination, the structure incorporates $N-1$ combiners with progressively increasing coupling factor form 3 to $10.log_{10}(N)$ and delay lines (phase shifters) to properly equalize the phase of the traveling signals in the different paths. As a result, for a N-stage combiner, each successive stage adds $1/N$ of the output power.

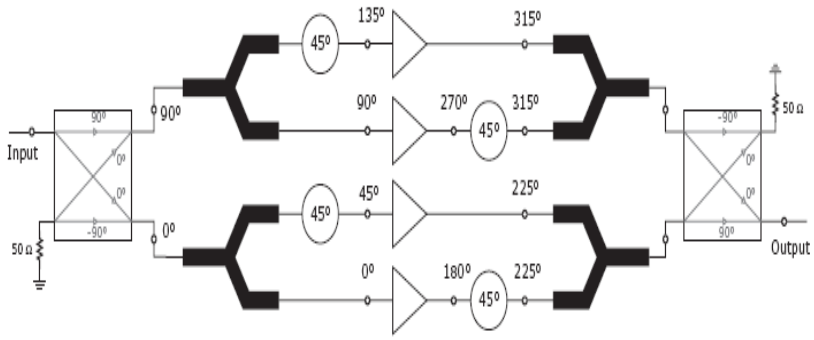


Figure 9.18: Mixed Hybrid/Wilkinson Corporate Structure

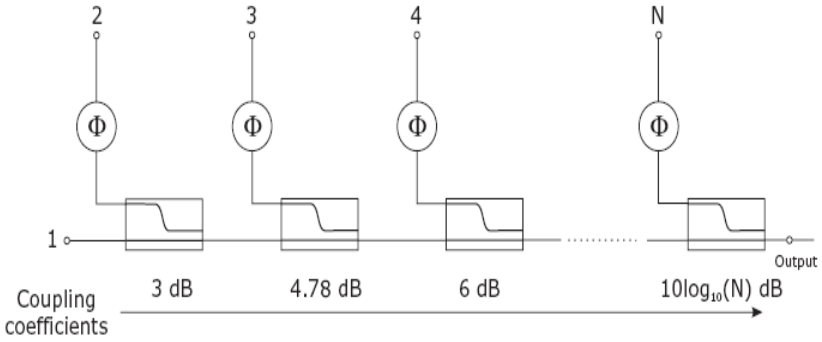


Figure 9.19: Travelling wave Combiner Structure Structure

In a real implementation the insertion loss of each coupler needs to be added the theoretical coupling factor in each stage. Again, Wilkinson combiners are excellent candidates for monolithic application due to its inter port isolation, inherent broadband and planar implementation. See for example [301] and [302]. Coupler could also be realized with lumped components approaches, even if resulting in a bandwidth reduction of the combiners. The later is really important since many foundry process allows lumped component implementation, thus reduction size in the combiner implementation con be achieved. The chain implementation is a non binary approach. This property shall be considered whit the first calculus related whit the necessary number of transistors in the output stage.
The number of stages is limited since is not easy to design high coupling factor couplers. Detailed calculation on combiner efficiency related the number of stages can be found in [289].

- **FEASIBILITY HINT:** Calculate optimum N and compare with other combining structures.
- **FEASIBILITY HINT:** Calculate the combining Efficiency in terms of number of combined devices and with a specific insertion loss per adder for each MMIC process.

9.3.4 Combination of Corporate/Wilkinson Combining Structures

One common solution to increase the output power (when high power is required) is to design chip of medium power (based on corporate structure) and combine the output power of each single chip using Wilkinson combiners. This configuration is commonly realized of chip, namely, Wilkinson combiners are implemented in printed circuit board. This last approach is called Hybrid since the final circuit is a combination of integrated circuits (MMICS or TRs) connected by means of micro strip/discrete circuits implemented in traditional printed circuit boards, (figure 9.20).

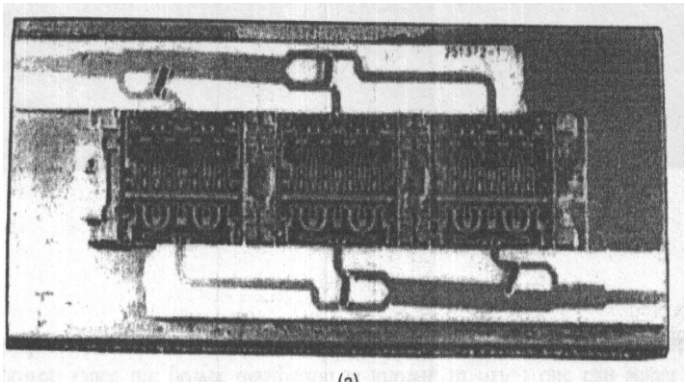


Figure 9.20: 12W High power Amplifier with Wilkinson combining of corporate PAs

The possibility of realize the overall circuit in MMIC fashion should be also considered. The main concern of this scheme is related with thermal issues and must be carefully calculated the trade-offs to decide on a final Hybrid or MMIC circuit.

- **FEASIBILITY HINT:** A mixed combination of corporate and Wilkinson combiner trade-offs would be carried out depending of the output power requirements.
- **FEASIBILITY HINT:** A study of trade-offs between Hybrid and MMIC structures would be carried out depending of the output power requirements.

9.3.5 Power Combining Efficiency

The *c*ombining efficiency is defined as he ratio between the combiner output power $P_{out,comb}$ and total combiner input power $P_{in,comb}$:

$$\eta_{comb} = \frac{P_{out,comb}}{P_{in,comb}} \tag{9.4}$$

Combining efficiency is one of the most important parameter to be considered deciding on what type structure must be used and shall be evaluated carefully in this work.
Combining efficiency depends on three factors:

- losses in combiner structures [24], [287].
- imbalances of the input signals [24].
- phase errors in signals being summed [24].

The effect of imbalances and phase errors were detailed studied in [303].

9.3.6 Graceful Degradation

Graceful degradation means that the power amplifier do not fail completely when one of its N active devices fails. A power amplifier based on power combining structure has the advantage of degrades its output power in a gradual fashion which makes this types of structure very attractive for high reliability applications (e.g satellite applications).
The way in which output power (or combining efficiency) decreases and how the effects of a single transistor or amplifier failures affect the overall performance was analyzed in [304], [305] and [306].

- **FEASIBILITY HINT:** Calculate and compare the robustness of combining structures in terms of relative number of device failures versus output power (or combining efficiency) in failure condition.
- **FEASIBILITY HINT:** Calculate output power (or combining efficiency) for the following four cases: Transistor input in short and open, transistor output in short and open [306].

9.3.7 Matching Issues in Power Combining

Another important aspect of the power combining process is related to the resulting influence on the impedance levels at the various section: suitable combining structures can be adopted to properly modify the output impedance of the overall structure [287].

Chapter *Matching* in this document presents a more detailed information in this subject.

- **FEASIBILITY HINT:** Overall output impedance shall be considered carefully in power combining structure selection.
- **FEASIBILITY HINT:** Calculate the overall output impedance in terms of individual active devices or power amplifiers output impedances.

9.3.8 Decision Making on Power Combining Structures

NOTE: The decision making at present work is driven primarily by reliability aspects leaving so far as a secondary matter the aspects related with die size (costs) or design engineering costs (circuit complexity).

The selection of a power combining structure shall be based mainly on the following criteria:

Primary Criteria:

1. Thermal Budget and Management (Reliability).
2. Graceful Degradation (Reliability).
3. Combiner Efficiency (Reliability).
4. Resistance to VSWR (Reliability).

Secondary Criteria:

1. Die Size (Cost).
2. Implementation Complexity (Cost).
3. Chip Repeatability (Cost).

To the end of this feasibility study a comparative table of above mentioned criteria shall be delivered. This table must present a comparison of each criteria (by foundry process) and a must contain a weighting function of each criteria to eases the decision making. The weighting of criteria would be modified in due course if required by CONAE.

NOTE: Highly Dependent of Foundry process information...

Chapter 10

Impedance Matching

This chapter presents a basic theory formulation for active device impedance matching, including equations, figures and references. The main intention is develop a minimum self contained material of the subject under study that serves of guidance during the feasibility study and also be useful for discussion template between involved organisms (IIIE -CONAE).

The material presented in this Chapter is thought to support concepts related to the *Design Strategy* aspect presented in chapter 2 (First Deliverable Document).

The chapter is organized as follow: First we review the Bode-Fano theoretical limits of matching circuits in function of the number of matching sections to have a priori dimension of matching capabilities according to the bandwidth requirements. Also is included a description of input and output Q factors of a standard microwave transistor. Second, we describe the main features of matching networks realized with lumped and transmission line components to have an idea of how this circuits may affect the overall design. Finally we present an overview of transmission line and matching concepts and equations to self contain the main theoretical aspects of the subject.

10.1 Introduction

The matching network circuits basically adapts the load impedance and generator impedance to the system impedance (or reference impedance) which is commonly 50Ω. The applications under study have a defined frequency bandwidth of operation which means that, the matching network circuit not only must adapt the central or carrier frequency, but also the entirely bandwidth. Thus, the simple concept bandwidth comes to play since, is quite different to match a *narrow band* circuit than a *broad band* circuit. Roughly speaking a narrow band circuit is when $Q_{Circuit}BW < 0.5$ [307], here $Q_{Circuit}$ is the quality factor of the output circuit (namely the transistor or amplifier) and BW is the required operating bandwidth and is defined as follow:

$$BW = \frac{(f_{High} - F_{Low})}{\sqrt{F_{High}.F_{Low}}} = \frac{(f_{High} - F_{Low})}{f_0} \tag{10.1}$$

f_0 the carrier frequency,
and $Q_{Circuit}$ is defined as:

$$Q_{Circuit} = 2\pi.f_0RC \tag{10.2}$$

Where, in the most simple case, R and C are the output device resistance and capacitance components respectively.

10.2 Fano-Bode Limits

So, the classic matching problem is one that Bode [308] and Fano [309] studied separately and states *h*ow to match a circuit with a defined $Q_{Circuit}$ to a required bandwidth (BW) constrained by the maximum permissible reflection coefficient magnitude Γ_m and for a given number n of tuned circuits (or stages) in the impedance matching circuit.
The relationship between above mentioned circuit parameters is as follow (see [24] for details):

$$\Gamma_m = e^{-\pi.Q_{Circuit}/BW} \tag{10.3}$$

Figure 10.1 shows the Γ constraint concept for the ideal case of optimum reflection coefficient in the entire band BW.

Following, Bode [308] first determined the relationship between $Q_{Circtuit}$, BW and Γ for the theoretical case of infinite number of tuned circuits:

$$Q_{Circui}.BW_\infty = \frac{\pi}{ln\left(\frac{1}{\Gamma}\right)} \tag{10.4}$$

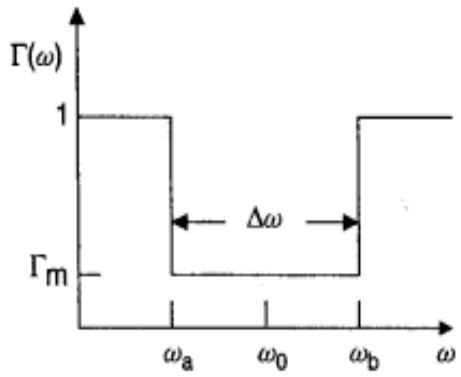


Figure 10.1: Optimum reflection coefficient for a given matching transformer

After that, Fano [309] determined the relationship between $Q_{Circtuit}$, BW and Γ for any number of tuned circuits. Below we present the first three cases which are mostly used:

$n = 1$,

$$Q_{Circuit}BW = \frac{2\Gamma}{1-\Gamma^2} \tag{10.5}$$

$n = 2$,

$$Q_{Circuit}BW = \frac{2\sqrt{\Gamma}}{1-\Gamma} \tag{10.6}$$

$n = 3$.

$$Q_{Circuit}BW = \frac{\sqrt{\Gamma}}{1-\sqrt{\Gamma}} \tag{10.7}$$

To better understating of the above relationships (10.5, 10.13, 10.7 and 10.4) let take a look to the next figure where for convenience Γ is plotted in terms of Return Loss in dB (see Equation 10.20):

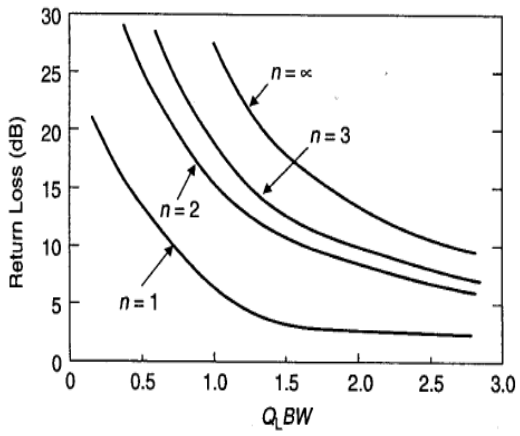


Figure 10.2: $Q_{Circuit}.BW$ product versus return loss for different tuned matching networks.

It is clear from Figure 10.2 that certain bounds of return loss (or Γ) does exist and that beyond the three sections of tuned stages in matching circuit, its value do not improves significantly if we increase the number of stages (3 sections bound is quite close to infinite sections bound). This gives us a reference of the matching circuit complexity we could expect with the requirement values of $Q_{Circuit}$, BW and Γ_m at hand.

- **FEASIBILITY HINT:** Calculate the minimum number of matching sections to verify BW and Γ specifications in function of a given maximum breakdown voltage or VSWR.

10.3 Typical Q expression for Transistors

Previous sections we mention the feature $Q_{Circuit}$ which depends on R and C of the output circuit. In fact, the transistor is a bilateral devices meaning that not only the output impedance play a role in the circuit but also the input impedance. In power amplifier the input and output impedances are respectively:

10.3.1 Input Transistor's Q

Input resistance and input capacitance (C_{GS}, Gate-Source) are in series:

$$\frac{\Delta f_{in}}{f_o} = \frac{1}{Q_{in}} = 2\pi f_o R_{in} C_{in} \tag{10.8}$$

10.3.2 Output Transistor's Q

Output resistance and output capacitance (C_{DS}, Drain-Source) are in parallel:

$$\frac{\Delta f_{out}}{f_o} = \frac{1}{Q_{out}} = \frac{1}{2\pi f_o R_o C_o} \tag{10.9}$$

10.4 Matching Components

Matching component can be implemented either with transmission line components or with lumped components. As a rule of thumb when a component has a size of the order of $\lambda/20$ can be treated as a concentrated or lumped component (λ is the operating wavelength), otherwise if it is greater than this value it behaves as a transmission line [51].
Next figure 10.3 shows a general classification of matching components.

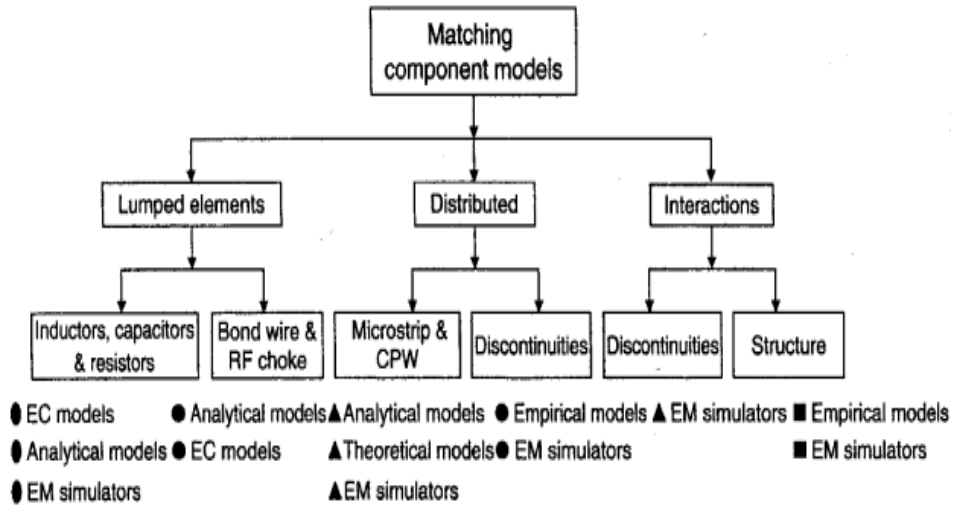


Figure 10.3: Overview of amplifier matching components

10.4.1 Matching with Transmission Line Components

Transmission line components are those constructed with transmission lines sections. For a transmission line structure to be suitable as a matching circuit element, one of the principal requirements is that the characteristics of the element can be determined from dimensions in a single plane. Micro strip lines are one of the basic building blocks of matching networks in MMIC circuits, see [310] for details.
The microstrip line is the most commonly used transmission medium in RF and microwave circuits, due to its quasi-TEM nature and excellent layout flexibility. Components realized with this technique are much smaller that wavelength, even more, in certain cases microstrip components can be used as a lumped components.

10.4.1.1 Insertion Loss

Losses in microstrips are caused by both, conductor loss and dielectric loss. The conductor loss (α_c) occurs due to finite resistance of the metal strip and ground plane, and the dielectric loss (α_d) is a result of the loss tangent of the substrate.
Below we presents closed forms in dB for conductor and dielectric losses:

$$\alpha_c = 0.072 \frac{\sqrt{f}}{W.Z_0} \tag{10.10}$$

where f is the operating frequency and W is the strip width and,

$$\alpha_d = 27.3 \frac{\epsilon_r}{\epsilon_r - 1} \frac{\epsilon_{re} - 1}{\sqrt{\epsilon_{re}}} \frac{tan\delta}{\lambda_0} \tag{10.11}$$

where λ_0 is the free space wavelength of f, $tan\delta$ is the loss tangent of the dielectric substrate and ϵ_r is the dielectric constant.
For RF and microwave substrates the conductor loss dominates and must be taken into account.

- **FEASIBILITY HINT:** Calculate the transmission line components values and the die size to implement them (foundry should provide as many data as possible).
- **FEASIBILITY HINT:** Calculate the insertion loss, at the output, of previous matching circuit.

10.4.2 Matching with Lumped Components

A lumped component in RF and microwave circuit is defined as a passive element whose size across any dimension is much smaller than the operating wavelength so there is no appreciable phase shift between the input and output terminals.
Capacitors: Can be implemented in microstrip, meal-insulator-metal (MIM) and inter digital. A small length of an open circuited microstrip section can be used as a lumped capacitor. MIM capacitors are fabricated using multilevel process and provide the largest capacitance. Inter digital are used when moderate high Q is required. A detailed treatment of these components can be found in [51].
Inductors: Can be implemented in two or three dimensions. Two dimensional inductors (or printed inductor) include a section if high impedance line, loop and coil. The coil may have rectangular, hexagonal, octagonal or circular shape. Three dimensional inductors consist of multiple layer of two dimensional inductors.
Resistors: Are implemented using transmission lines with lossy conductor materials such as NiCr or tungsten nitride resistive metal, the microstrip section behaves s a resistor since its resistive part becomes dominant.

10.4.2.1 Insertion Loss

The insertion loss depend of the function of each element, here we will not enter in not many details but says in general way that printed inductors should your losses to two factors: *substrate loss* and *metal layer loss*. The capacitor in any of their configurations have its own losses due to the loss tangent of the dielectric material. And finally the resistors causes losses mainly due to I^2R dissipated in themselves. Book [51] presents detailed aspects of lumped component design

- **FEASIBILITY HINT:** Select and calculate the lumped components values and the die size to implement them (foundry should provide as many data as possible).
- **FEASIBILITY HINT:** Calculate the insertion loss, at the output, of previous matching circuit.

10.4.3 Comparison between Microstrip and Lumped Elements

Table 10.1 summarizes the main characteristics of lumped and microstrip elements.

	Microstrip	Lumped
Advantages	Well characterized and has flexibility in design	Capable of transforming high impedance ratios
	Low loss and high performance	minimum interactions between element due to small size
	Has better harmonic tuning capability for high efficiency applications	Compact in size
Major disadvantages	Strong interaction effects between elements and discontinuities in packed design	Low Q, limited DC power handling capability
	Large in size even with interactions included	Substandard performance due to low Q at the output of a power amplifier in terms of Po and PAE

Table 10.1: Comparison of Distributed and Lumped Elements Matching Networks

10.4.4 Decision Making on Matching Network

NOTE: The decision making at present work is driven primarily by reliability aspects leaving so far as a secondary matter the aspects related with die size (costs) or design engineering costs (circuit complexity).
The selection of a matching network structure shall be based mainly on the following criteria:

Primary Criteria:

1. Thermal Budget and Management (Reliability).
2. Device Efficiency (Reliability).
3. Resistance to VSWR (Reliability).
4. Radiation Resistance (Reliability)

Secondary Criteria:

1. Die Size Implementation(Cost).

2. Design Complexity (Cost).

The deliverable at this point shall present a calculations in terms of availability of matching components, number of stages required (depending of process characteristics), complexity and insertion loss for each foundry process under study. The results shall be presented in a table to allow an easy comparison between foundry process. If were necessary on chip matching size must be compared with the same circuit implemented in PCB to determine the cost either, in a on-chip or off-chip

10.5 Review of Impedance Matching Theory

This section is for review purposes only.

- Reflection Coefficient with Phase, (Γ).
  (Γ is a complex variable)
  $$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{10.12}$$

- Reflection Coefficient Magnitude, (ρ).

  $$\rho = |\Gamma| = abs(\Gamma) \tag{10.13}$$

  It is easy to measure with power measurement but the phase is lost.

  $$\rho = \sqrt{\frac{P_R}{P_F}} \tag{10.14}$$

- Voltage Standing Wave Ratio, $VSWR$

  $$VSWR = \frac{(1+\rho)}{(1-\rho)} \tag{10.15}$$

  When, $Z_L < Z_0$, $VSWR = Z_0/Z_L$.
  When, $Z_L > Z_0$, $VSWR = Z_L/Z_0$.

- Relationship between Reflection Coefficient and $VWSR$

  $$VWSR = \frac{(1+\Gamma)}{(1-\Gamma)} \tag{10.16}$$

- Relationship between ($VWSR$) and the Reflection Coefficient

  $$\Gamma = \frac{(VWR-1)}{(VSWR+1)} \tag{10.17}$$

- Return Loss, (R_L)

$$ReturnLoss = R_L = 10 * log\left(\frac{P_R}{P_F}\right) \tag{10.18}$$

- Relationship between R_L,Γ and $VSWR$

$$R_L = -20log_{10}\left[\frac{VSWR - 1}{VSWR + 1}\right] \tag{10.19}$$

$$R_L = -20log_{10}(\Gamma) \tag{10.20}$$

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